

FIG. 1(a)

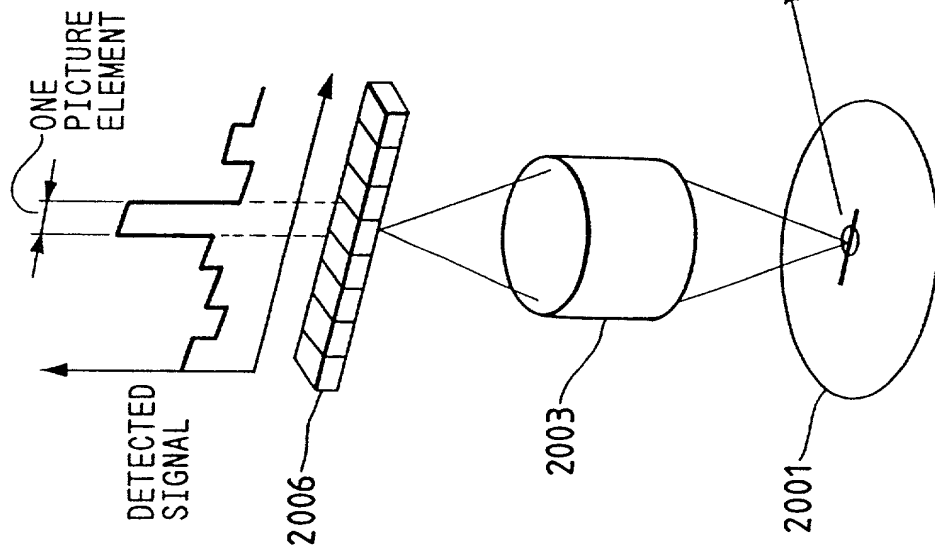


FIG. 1(c)

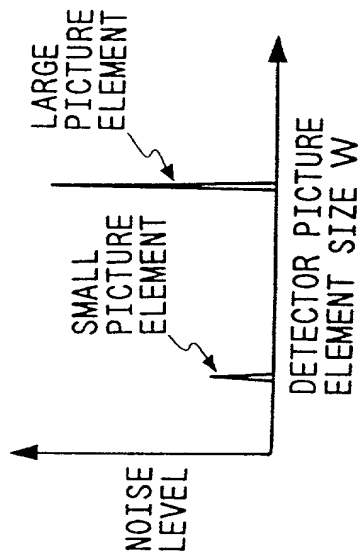


FIG. 1(b)

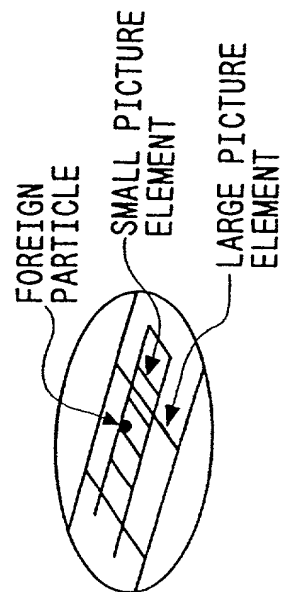


FIG. 2

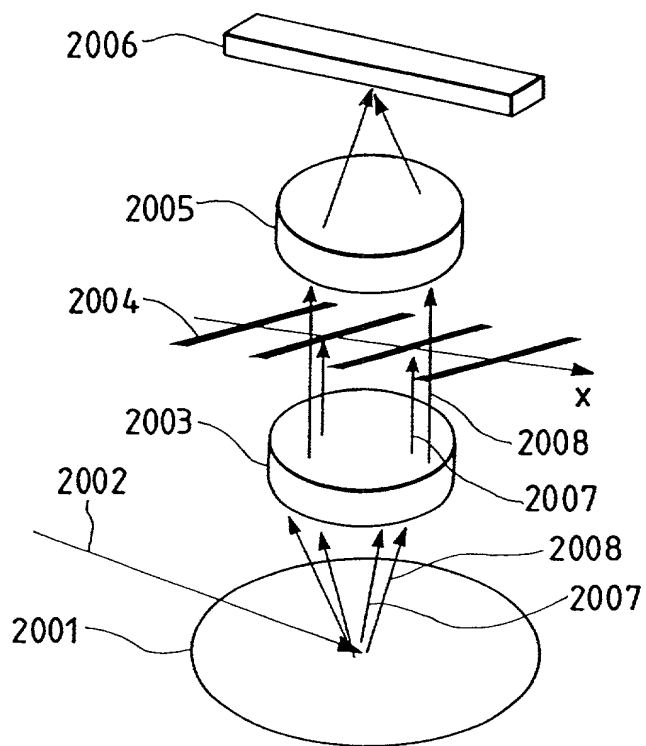


FIG. 3

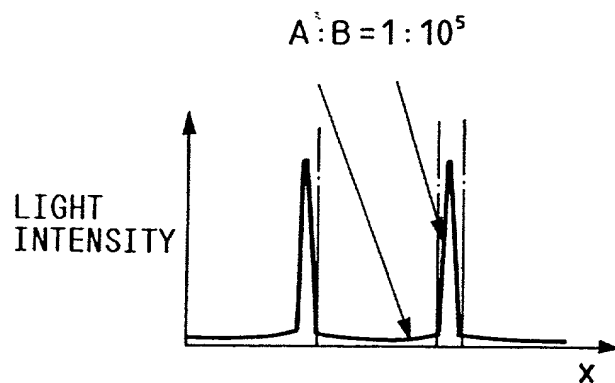


FIG. 4

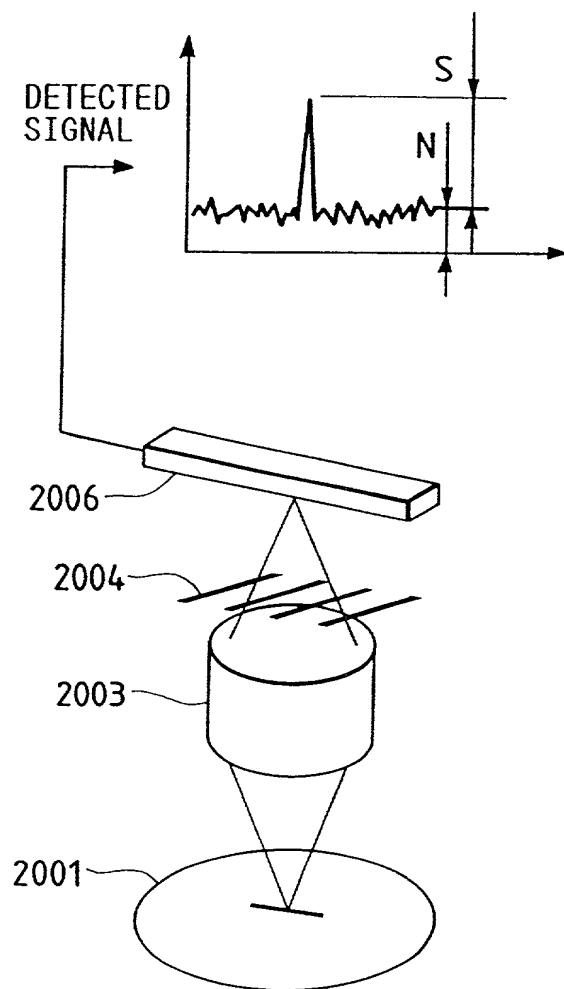


FIG. 5

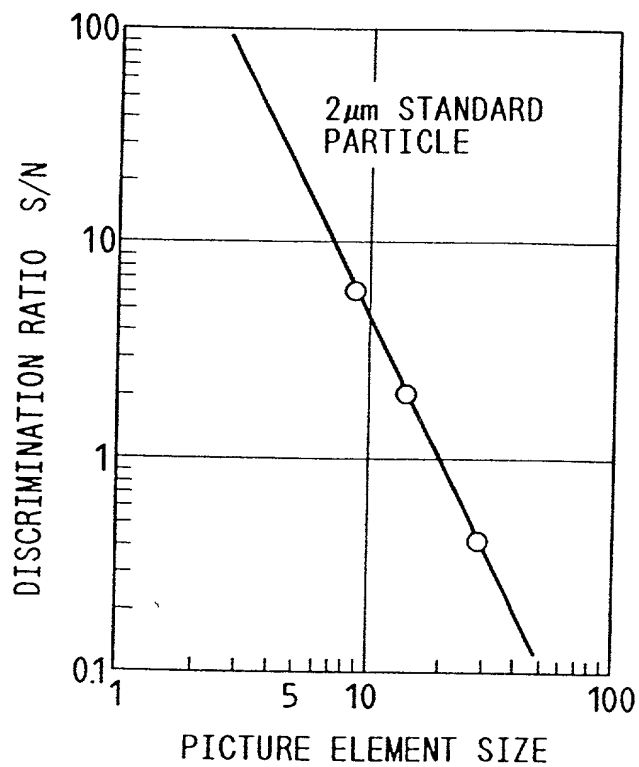


FIG. 6

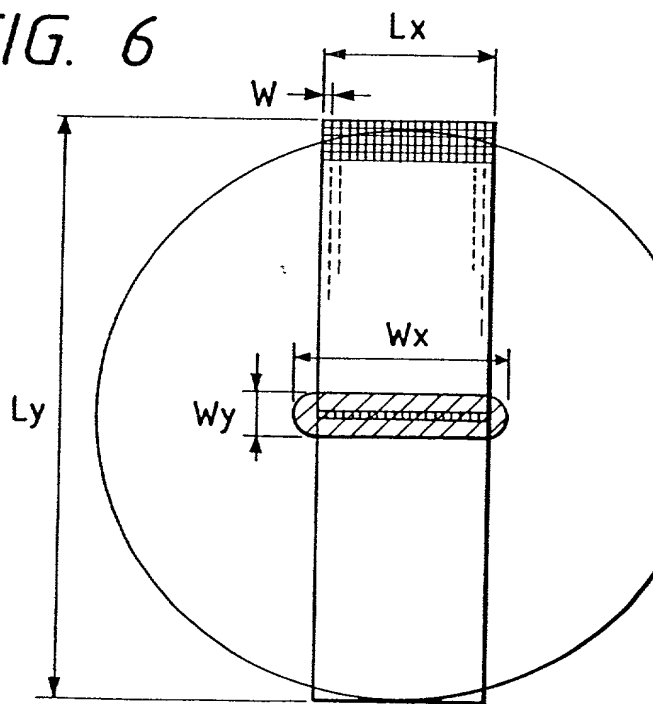


FIG. 7(a)

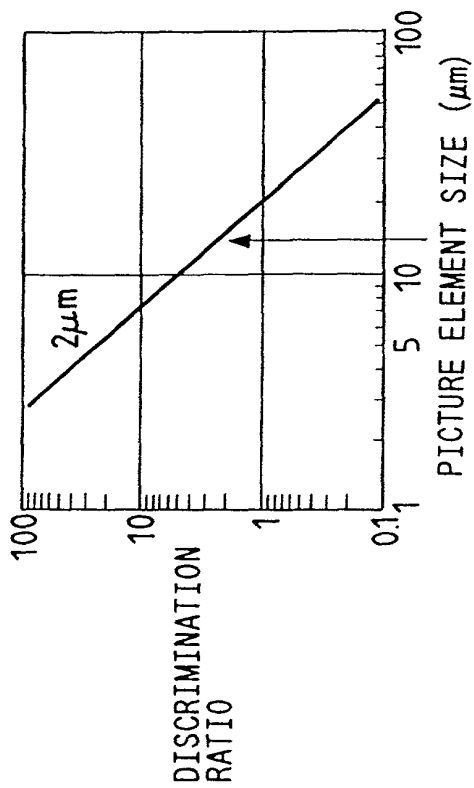


FIG. 7(b)

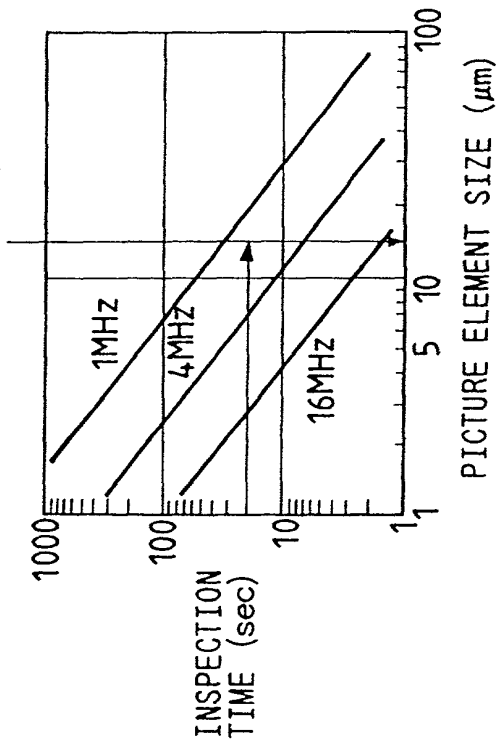


FIG. 7(c)

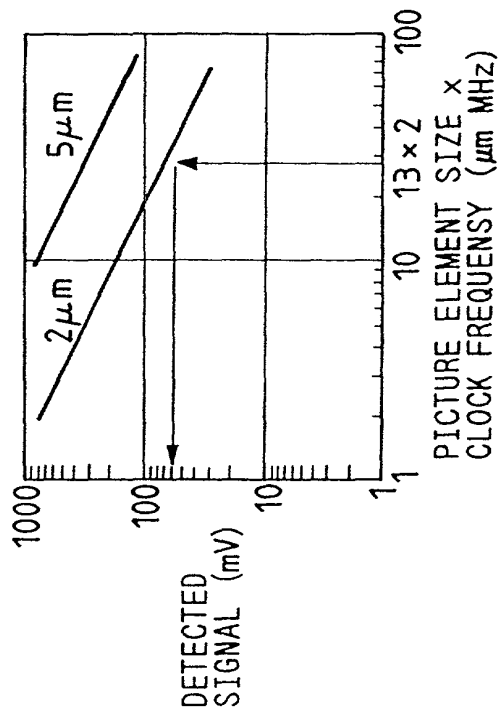


FIG. 8

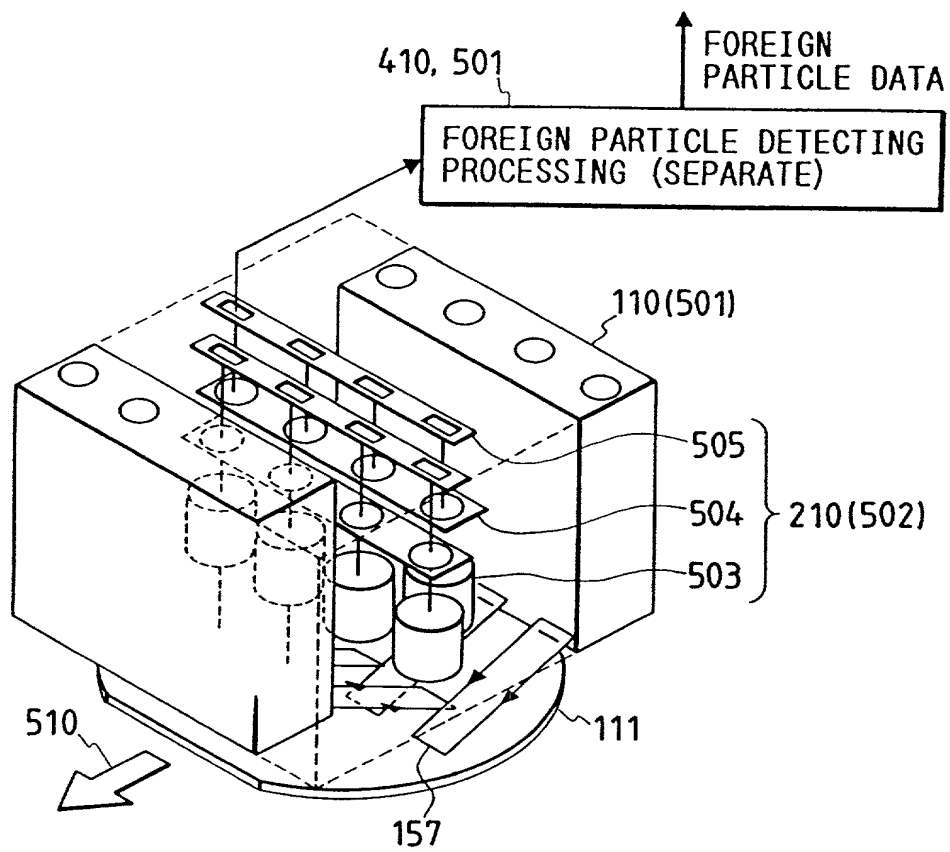


FIG. 9(a)

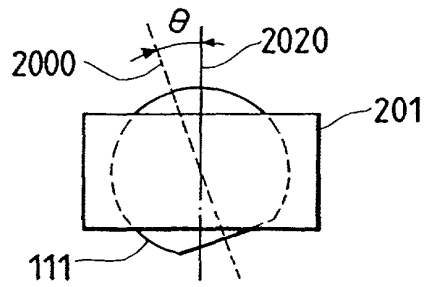


FIG. 9(b)

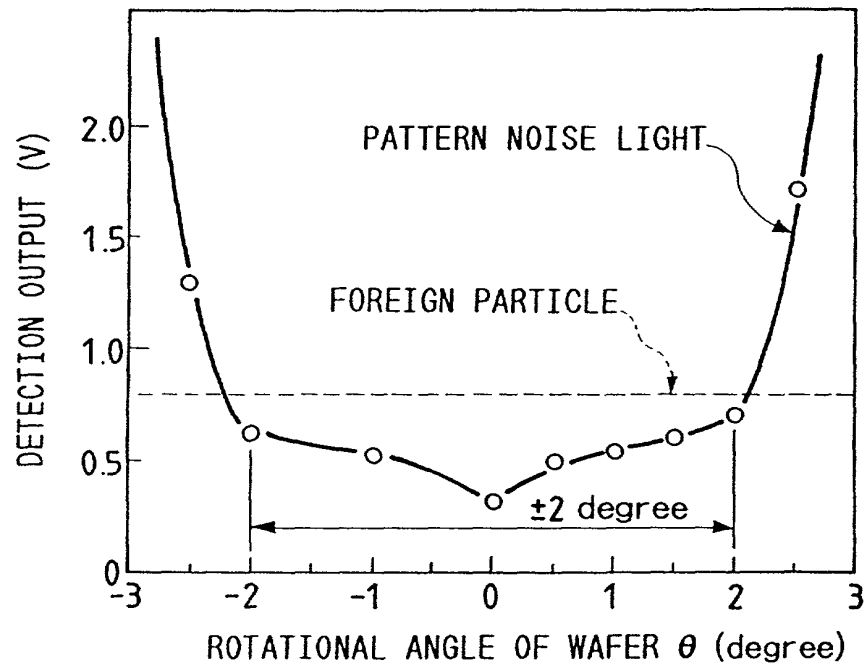


FIG. 10(a)

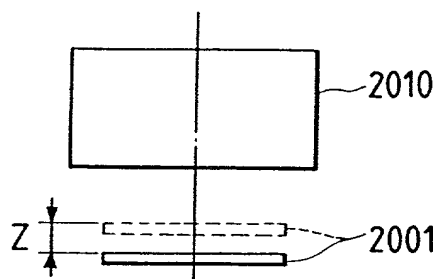


FIG. 10(b)

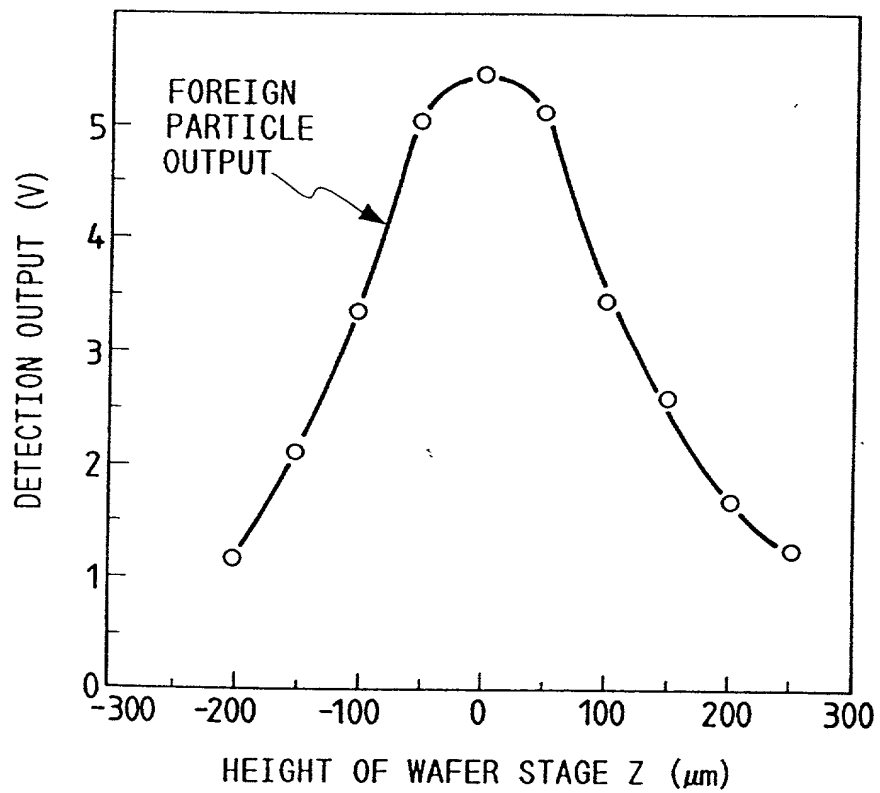


FIG. 11(a)

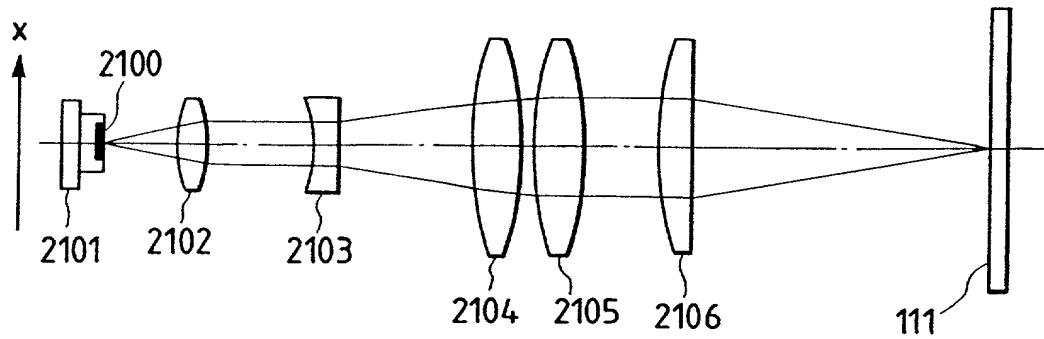


FIG. 11(b)

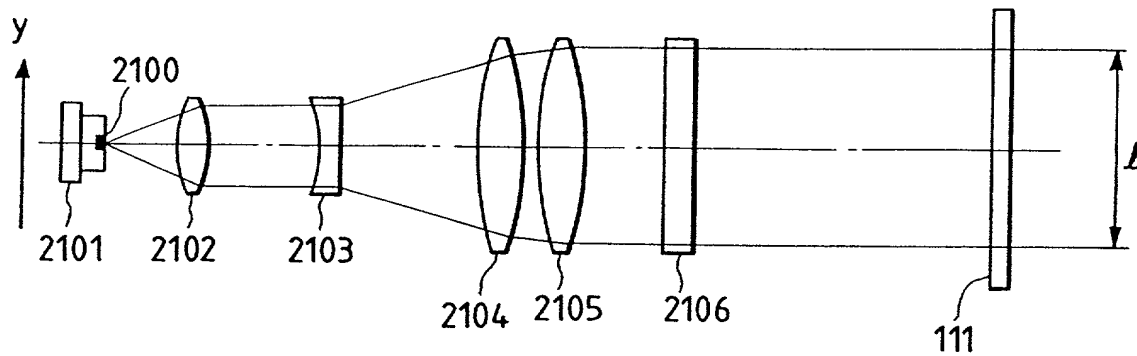


FIG. 12(a)

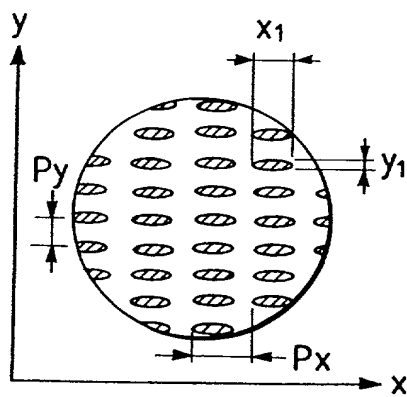


FIG. 12(b)

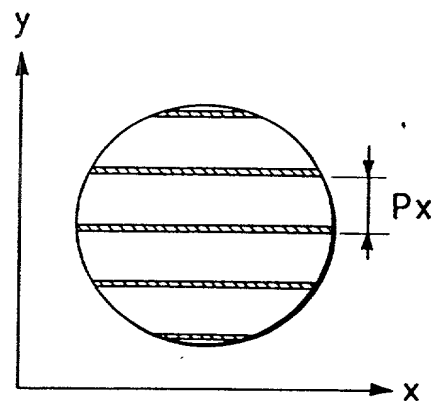


FIG. 13(a)

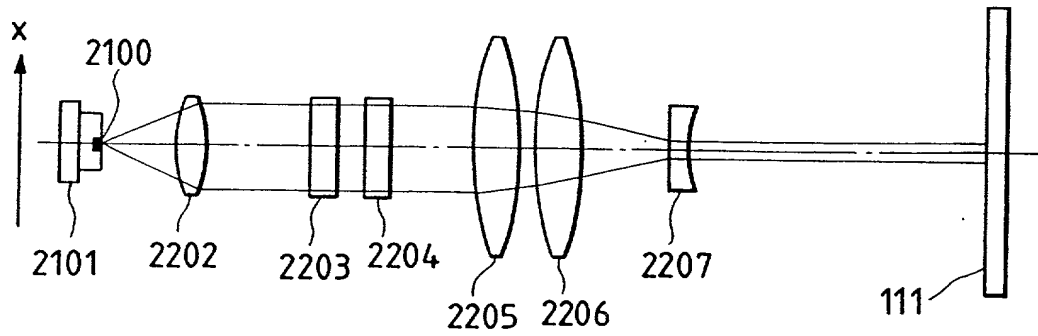


FIG. 13(b)

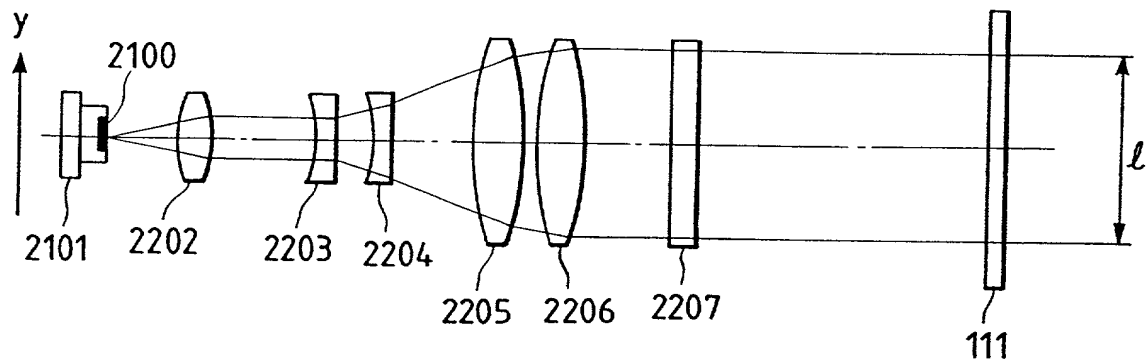


FIG. 14

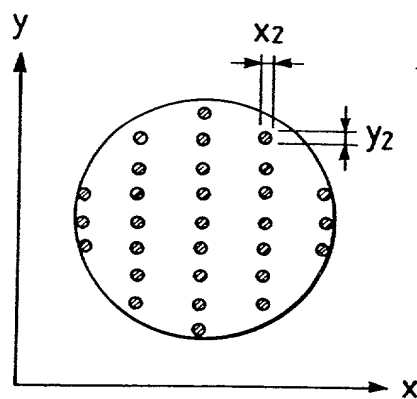


FIG. 15

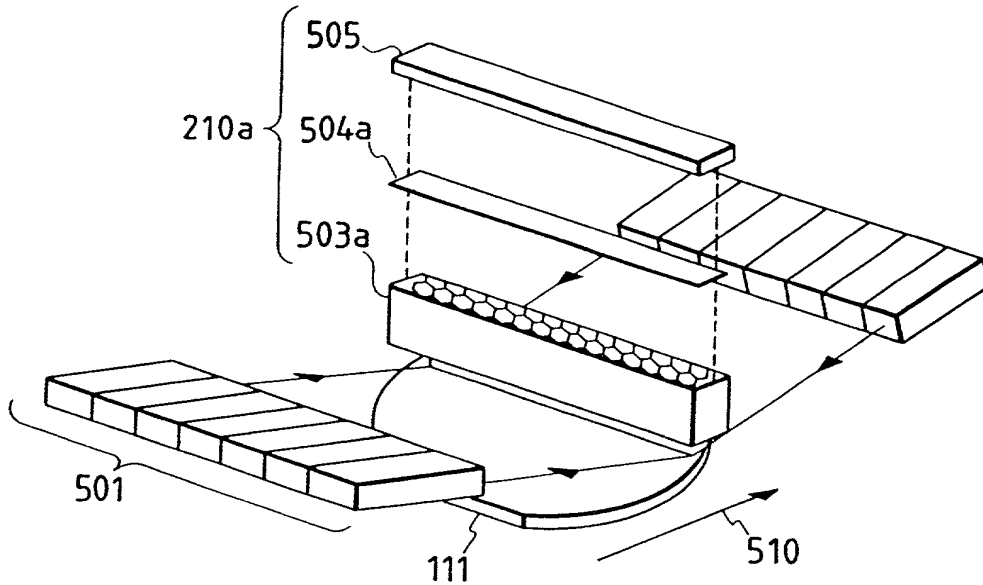


FIG. 16

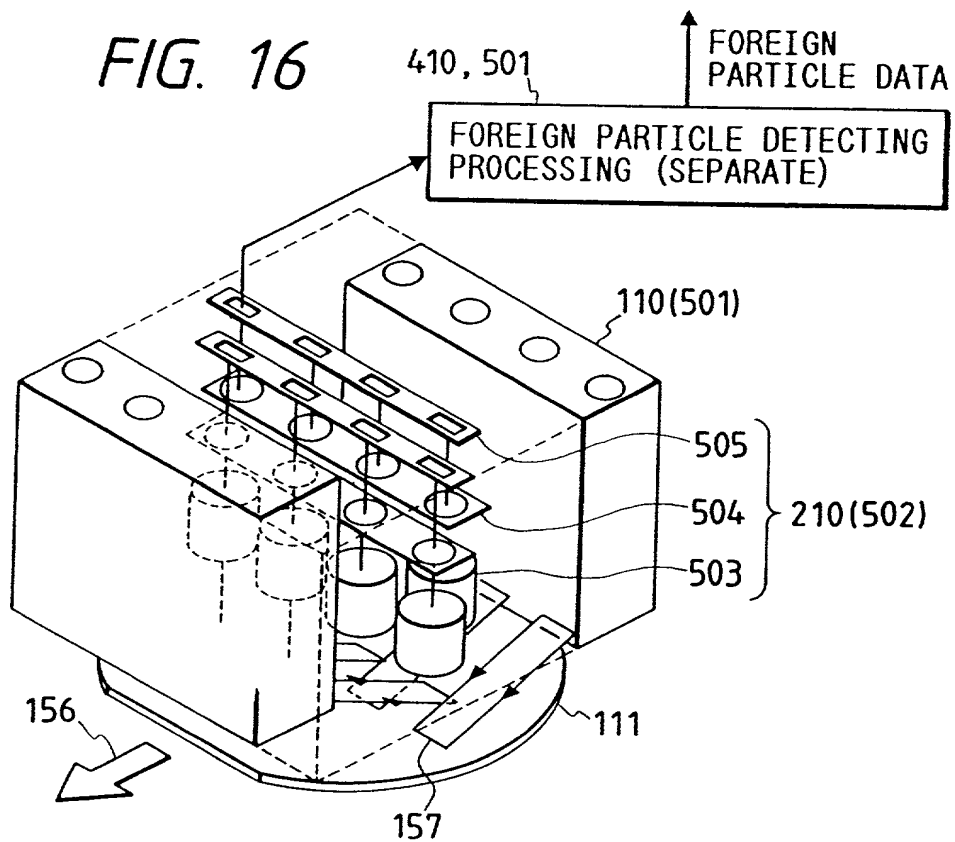


FIG. 17(a)

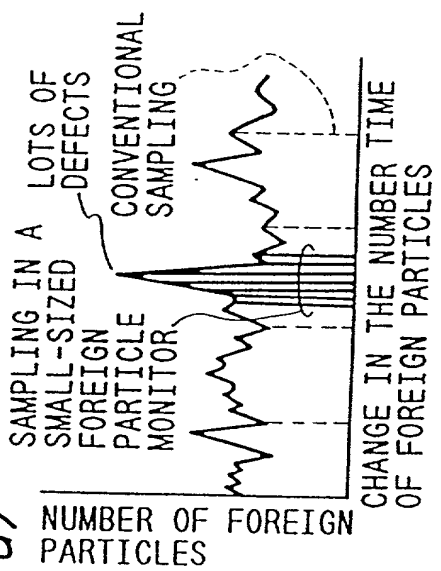


FIG. 17(b)

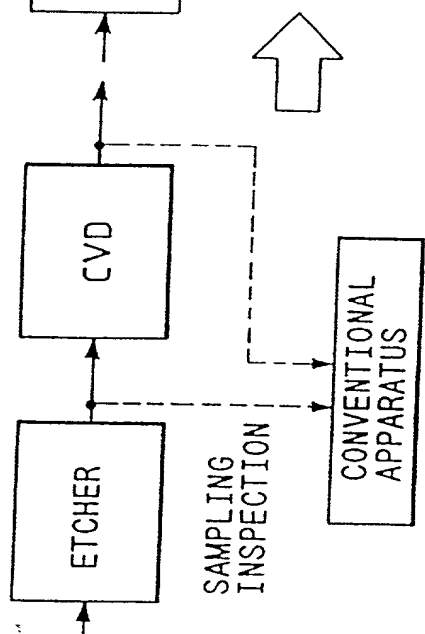


FIG. 17(c)

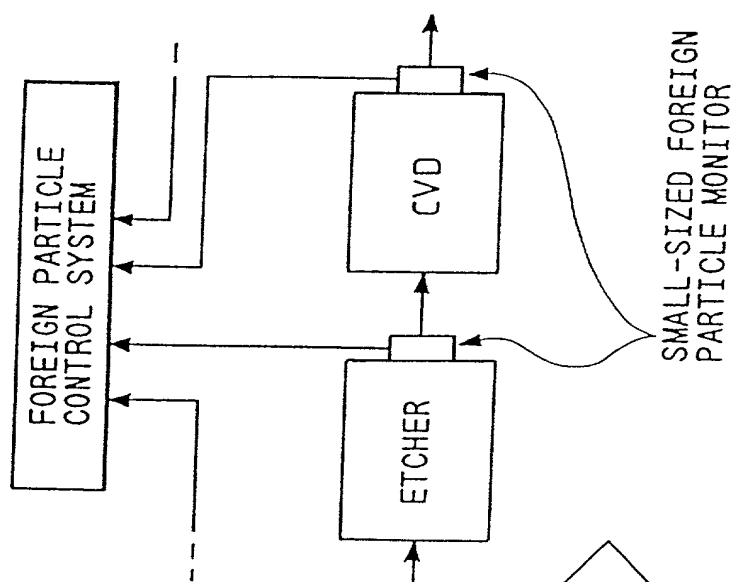


FIG. 18

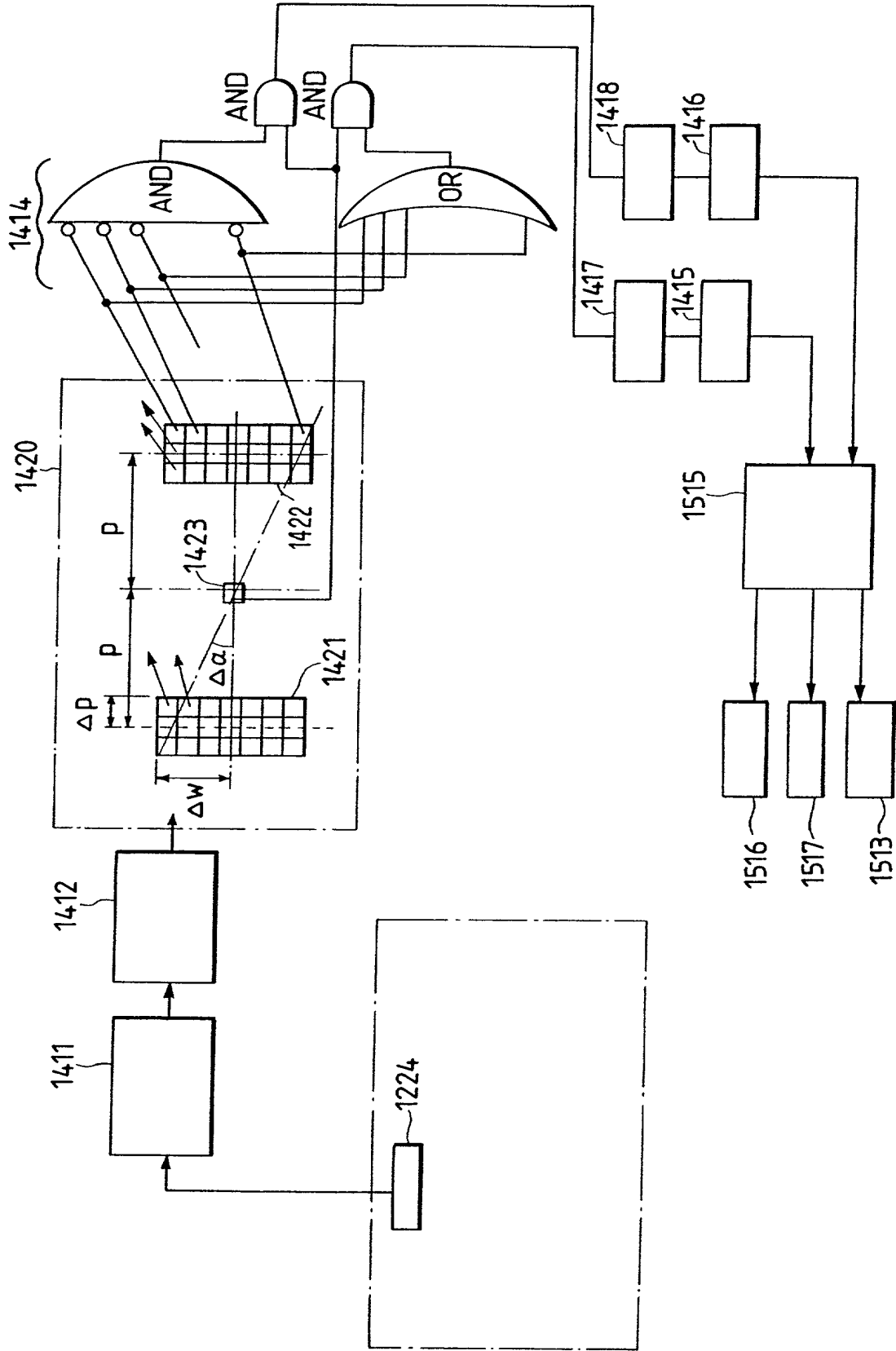


FIG. 19 is a block diagram of a system 1000. The system 1000 includes a processor 1100, a memory 1200, a network interface 1300, and a user interface 1400. The processor 1100 is connected to the memory 1200, the network interface 1300, and the user interface 1400. The memory 1200 is connected to the network interface 1300. The network interface 1300 is connected to the user interface 1400. The user interface 1400 is connected to the processor 1100. The system 1000 is configured to receive data from the user interface 1400, process the data using the processor 1100, store the data in the memory 1200, and transmit the data to the network interface 1300. The network interface 1300 is configured to receive data from the network and transmit the data to the user interface 1400. The user interface 1400 is configured to receive data from the network and transmit the data to the processor 1100. The processor 1100 is configured to receive data from the user interface 1400, process the data, and transmit the data to the network interface 1300. The memory 1200 is configured to store data received from the network interface 1300 and transmit the data to the processor 1100. The network interface 1300 is configured to receive data from the network and transmit the data to the user interface 1400. The user interface 1400 is configured to receive data from the network and transmit the data to the processor 1100. The processor 1100 is configured to receive data from the user interface 1400, process the data, and transmit the data to the network interface 1300. The memory 1200 is configured to store data received from the network interface 1300 and transmit the data to the processor 1100.

FIG. 19

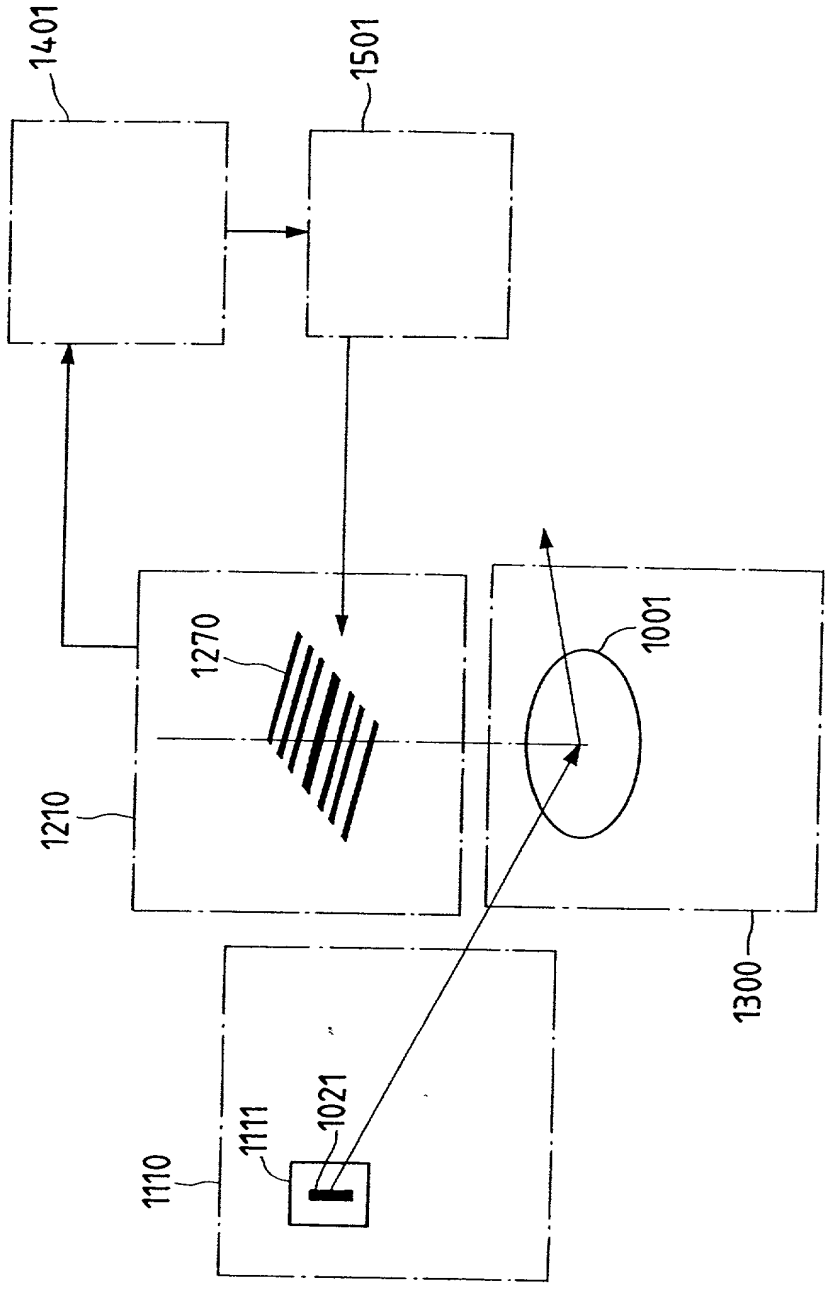


FIG. 20

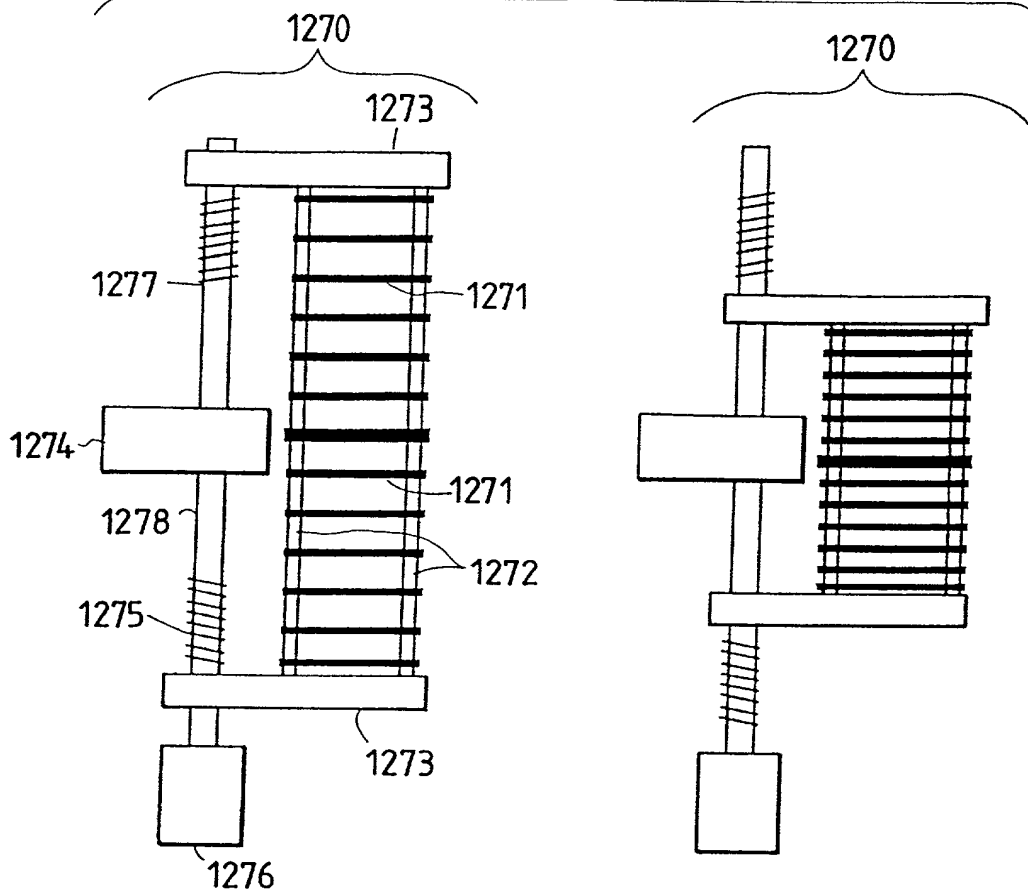


FIG. 21

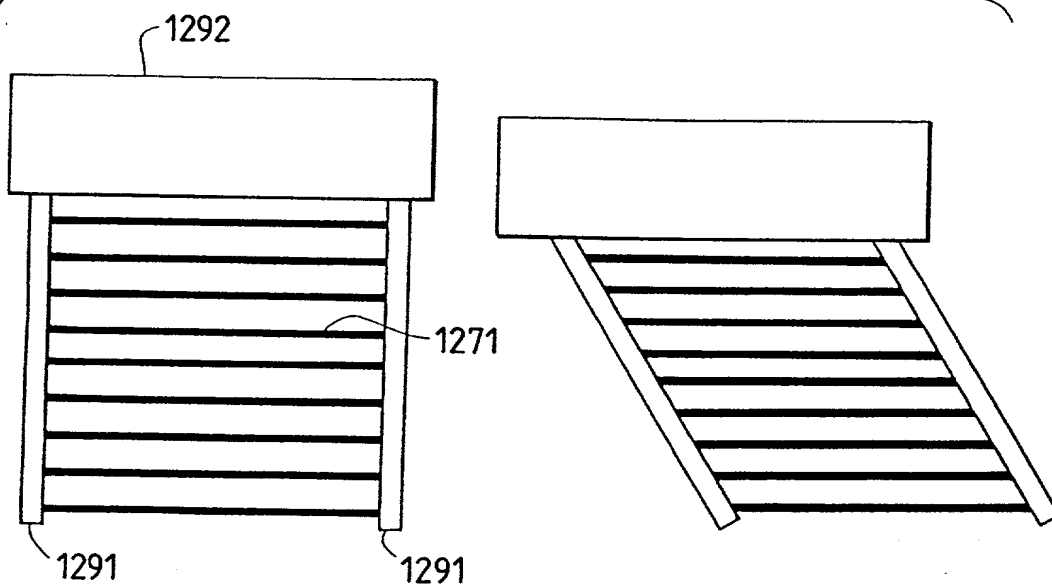


FIG. 22

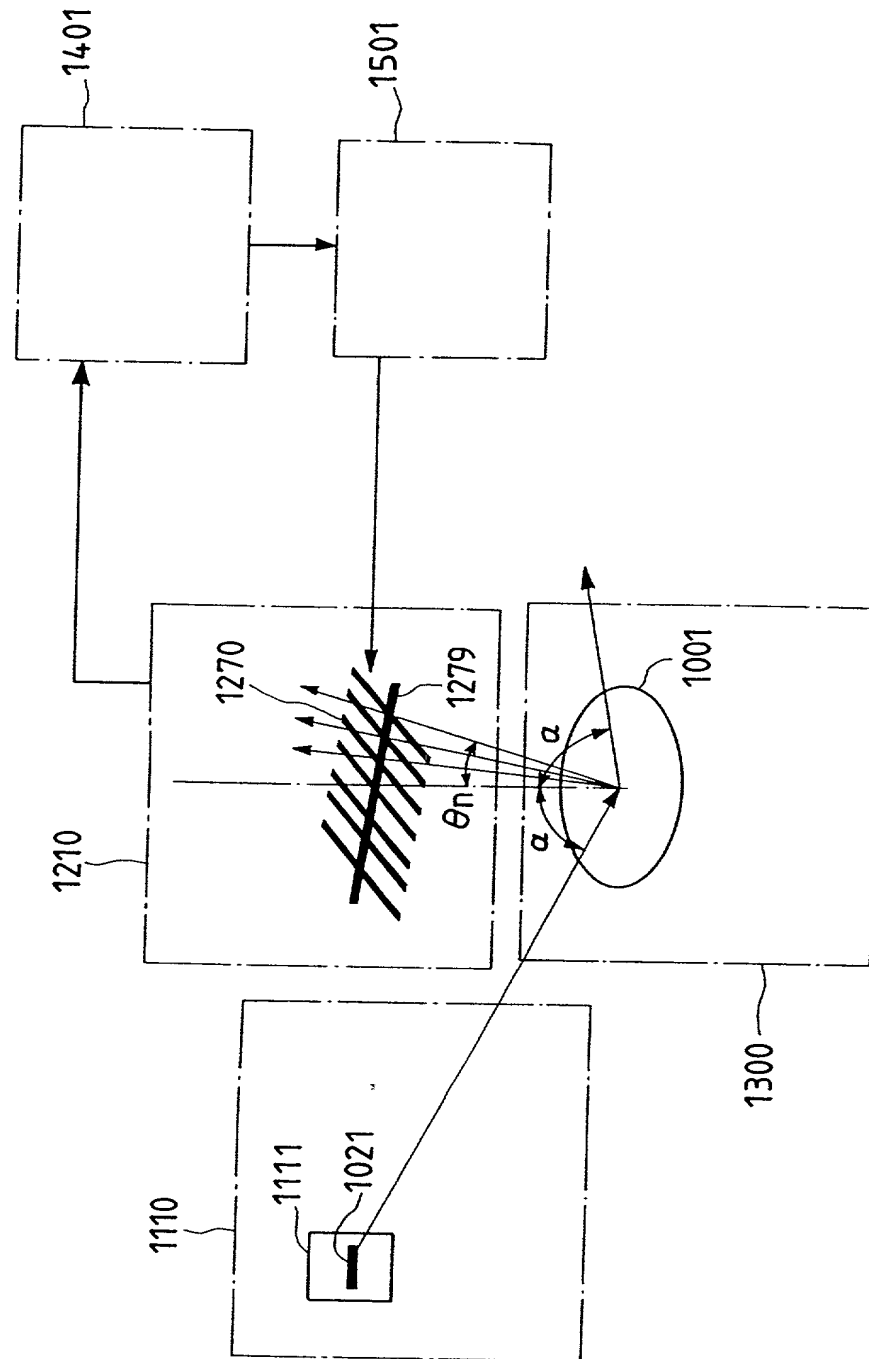


FIG. 23

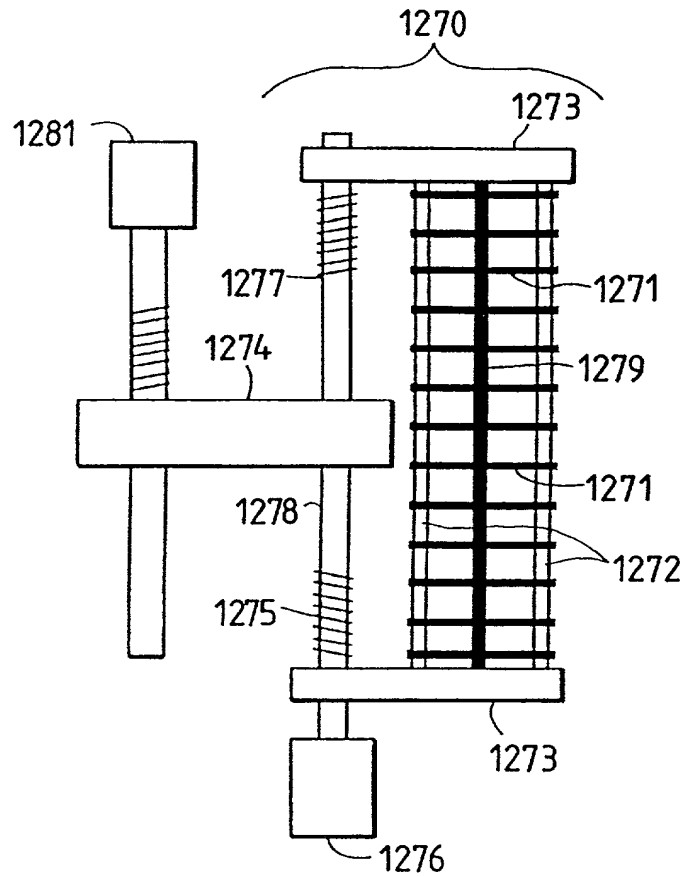


FIG. 26

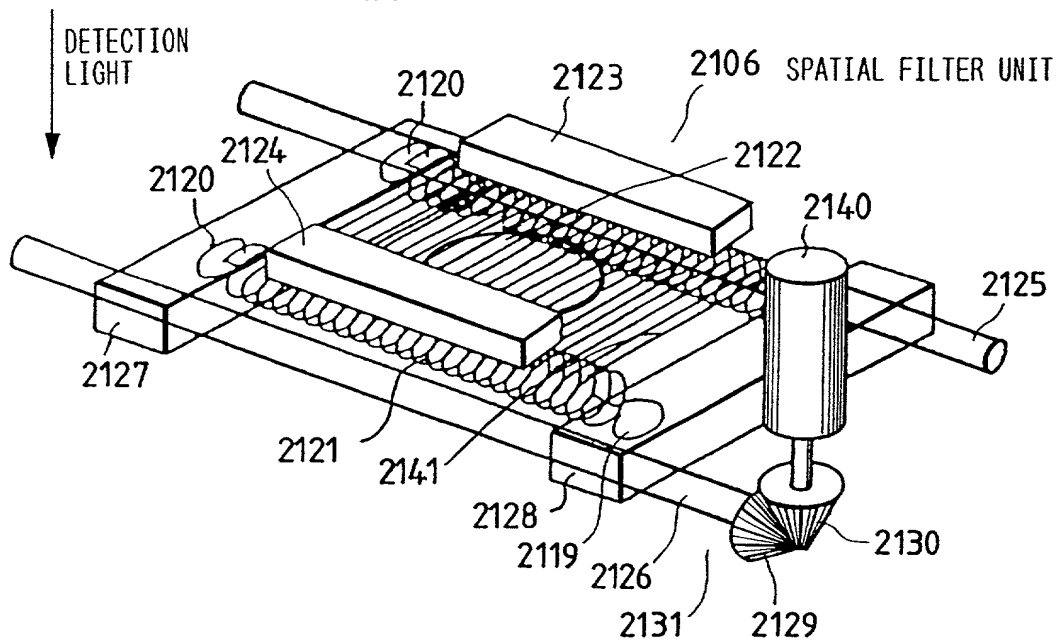


FIG. 24

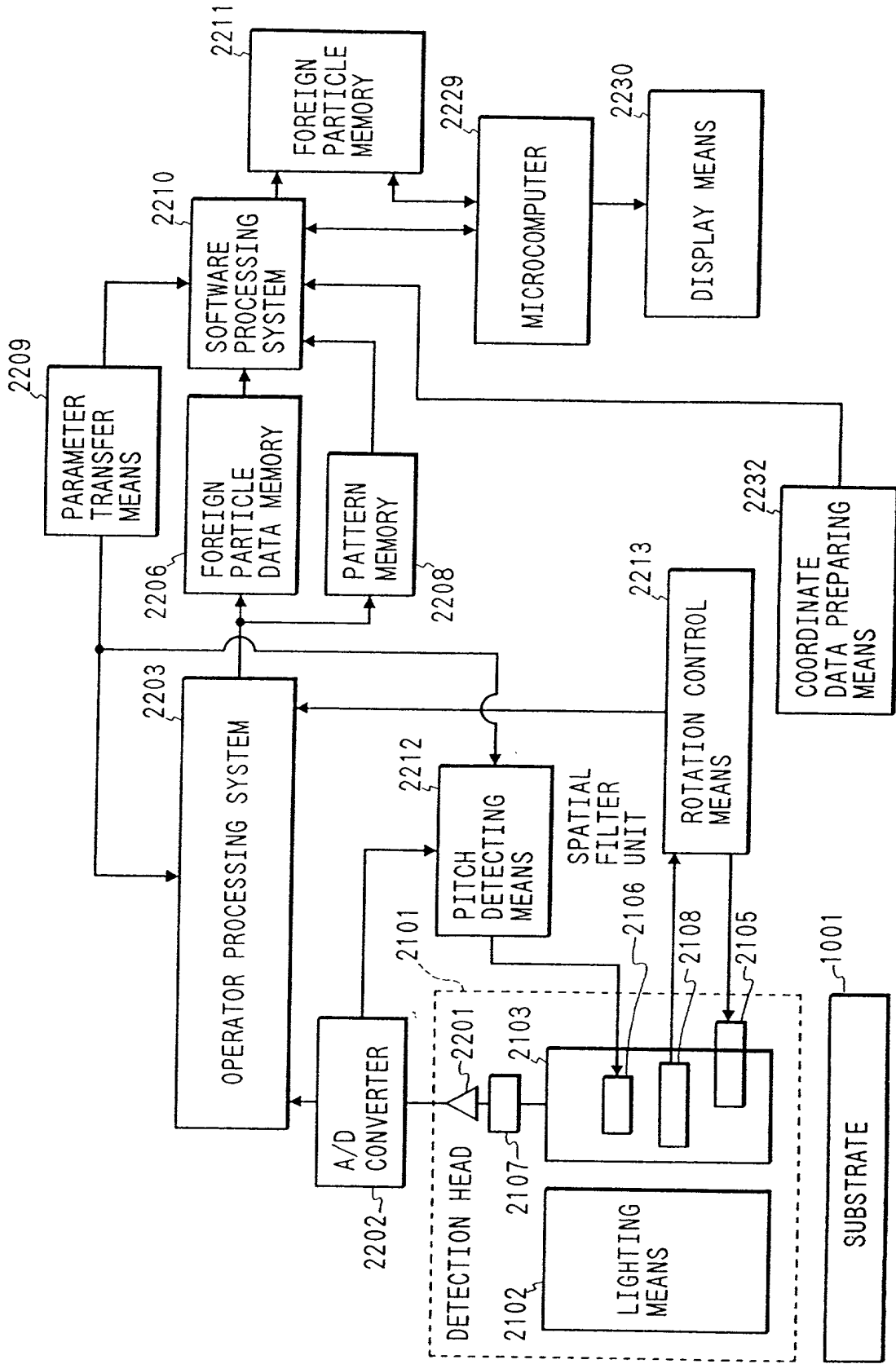


FIG. 25(a)

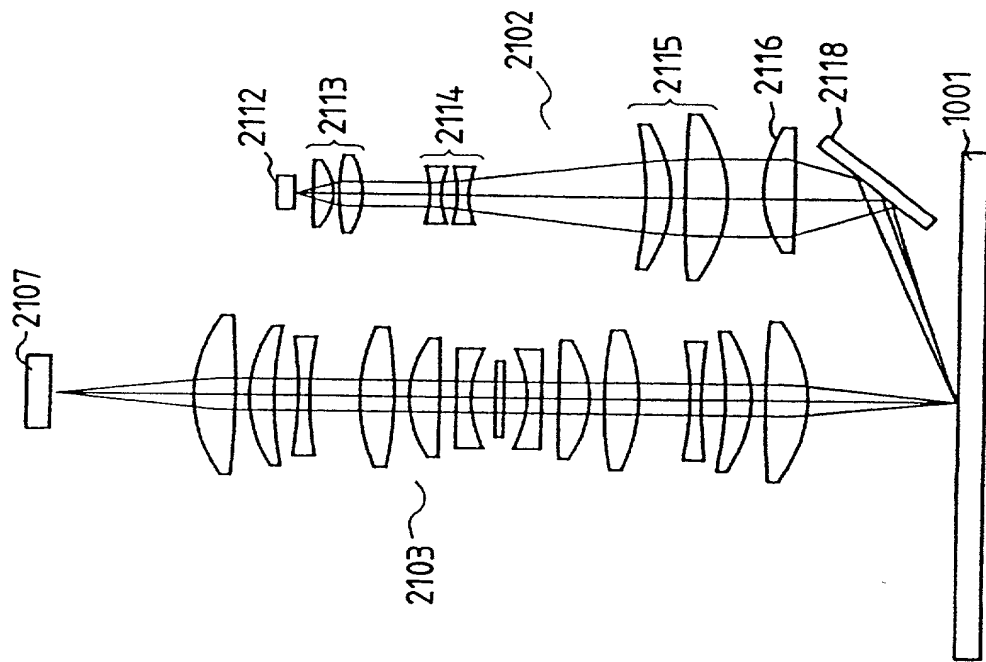


FIG. 25(b)

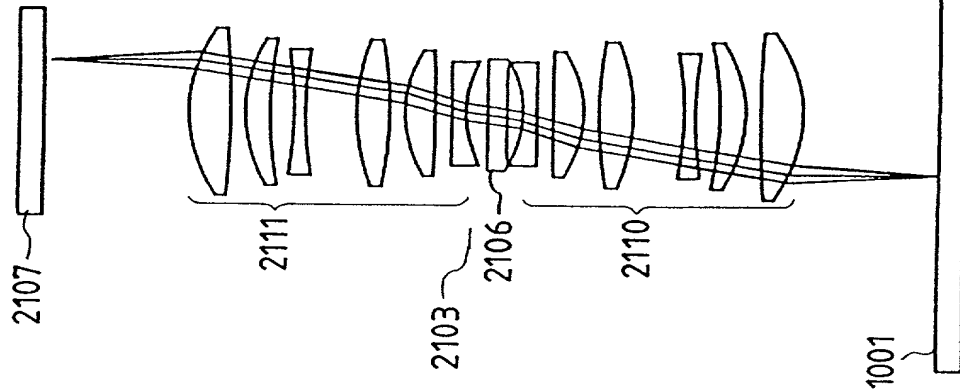


FIG. 25(c)

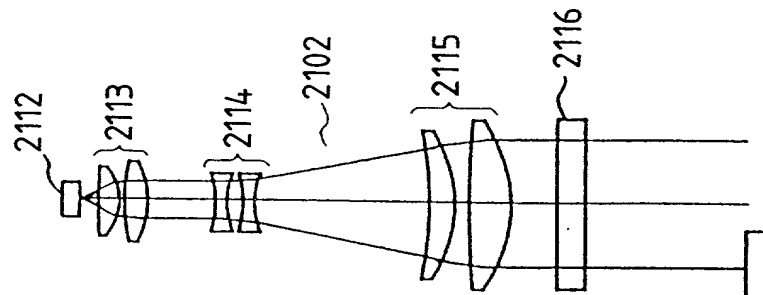


FIG. 27

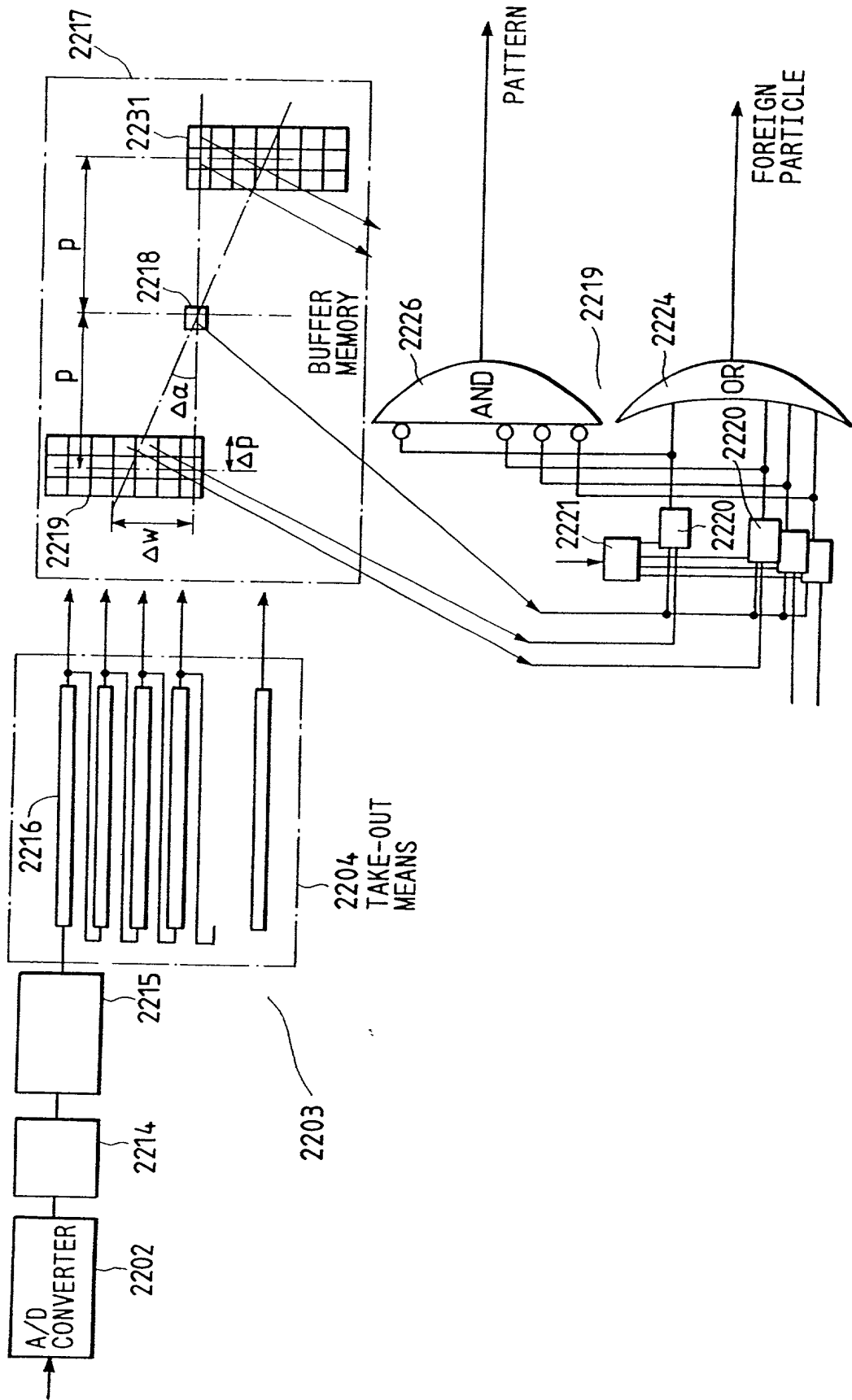


FIG. 28

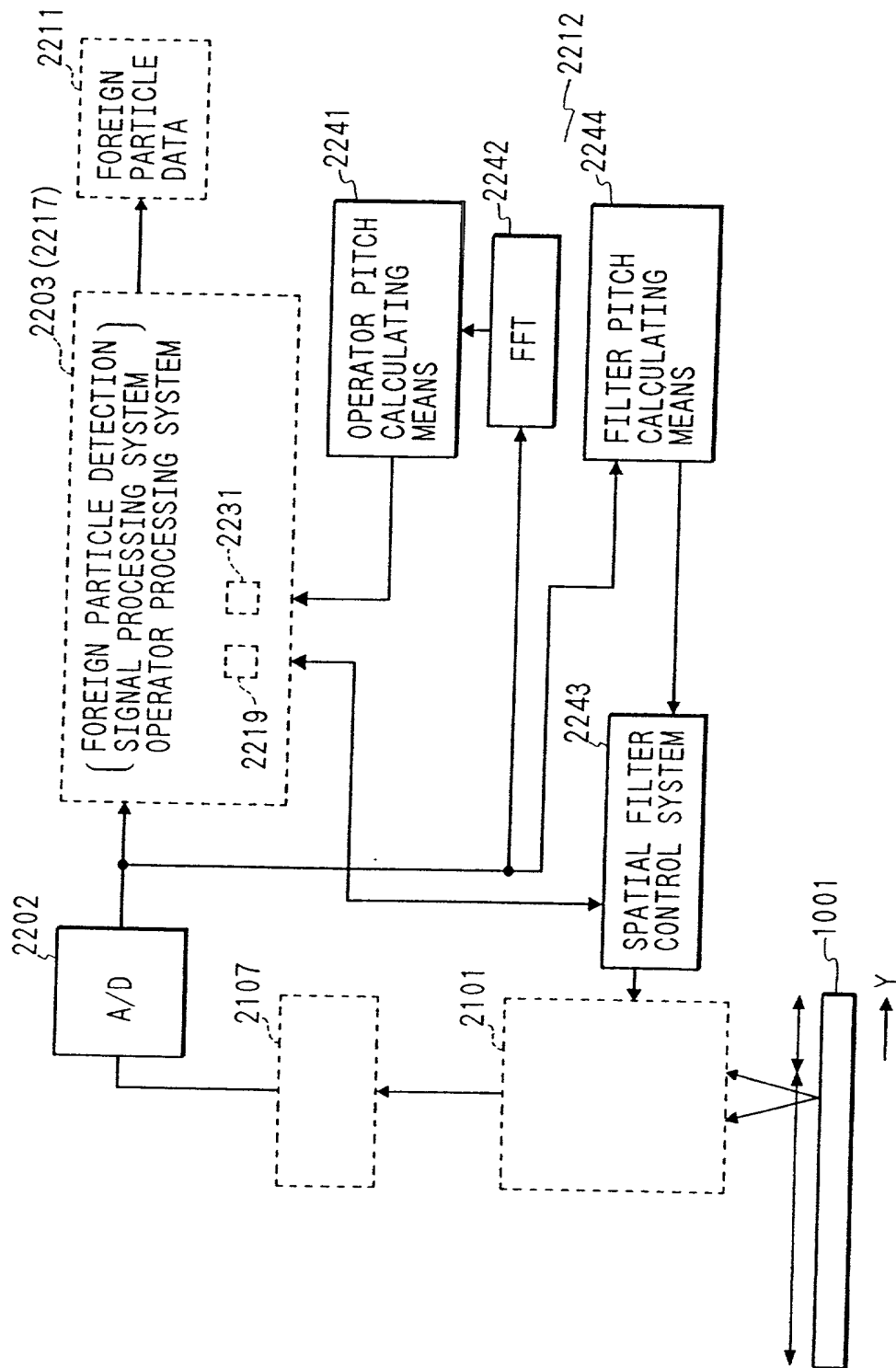


FIG. 29(a) PRIOR ART

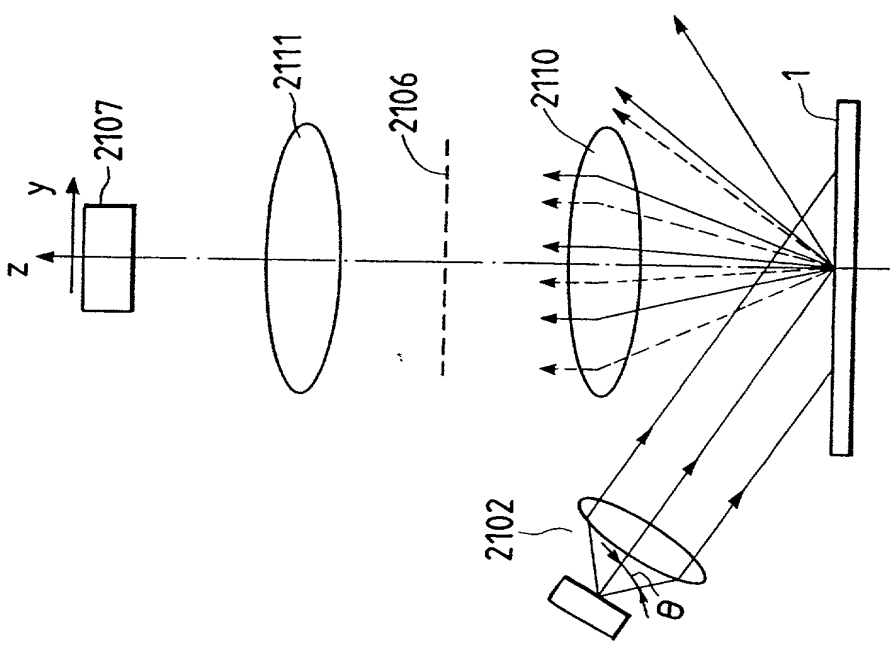


FIG. 29(b)
PRIOR ART

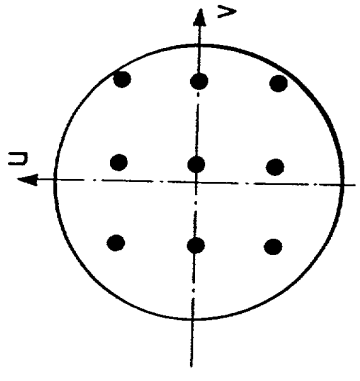


FIG. 29(c)
PRIOR ART

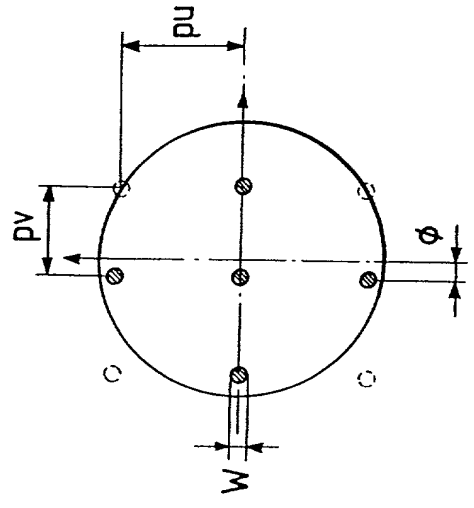


FIG. 30(a)

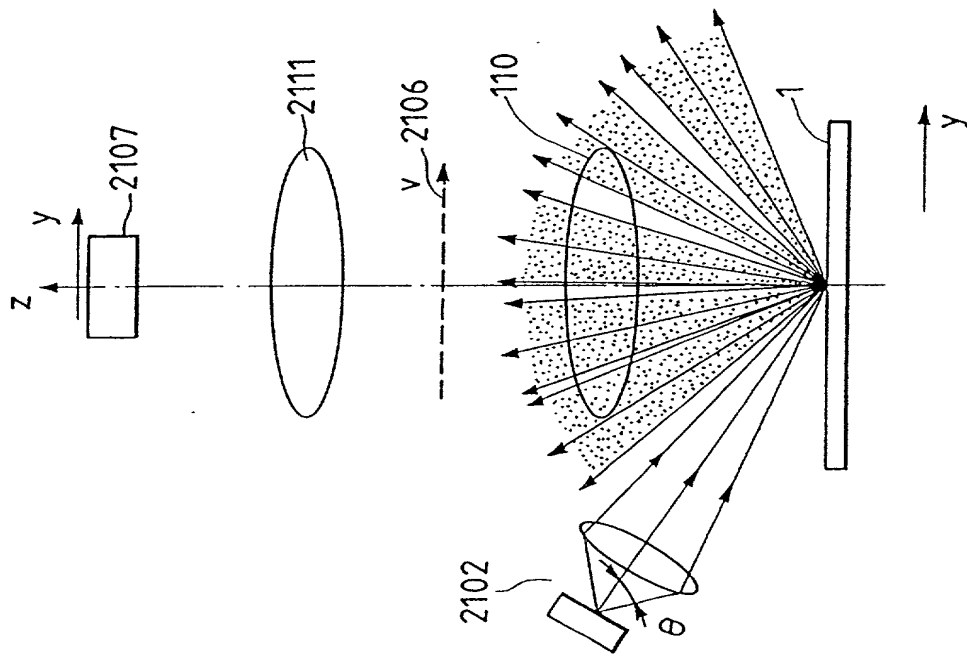


FIG. 30(d)

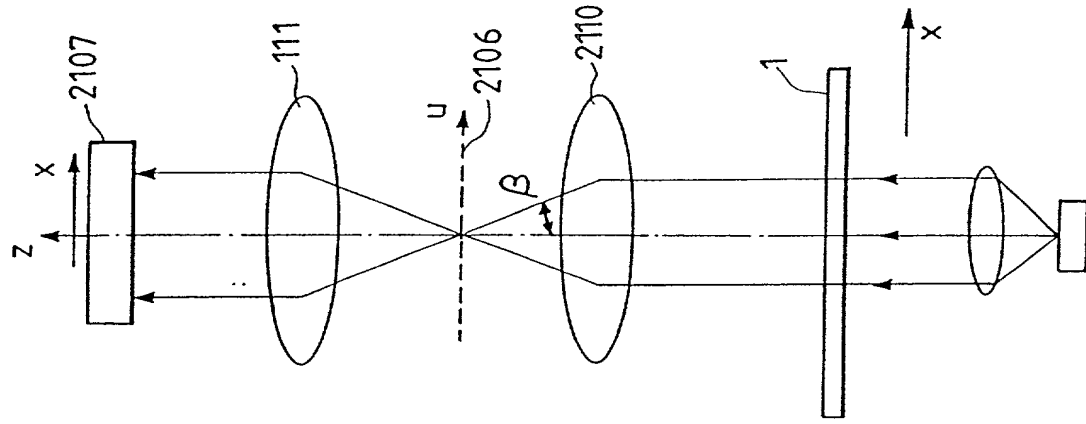


FIG. 30(b)

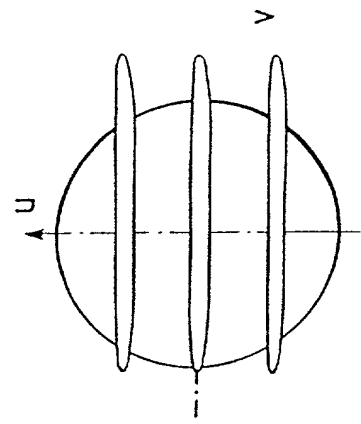


FIG. 30(c)

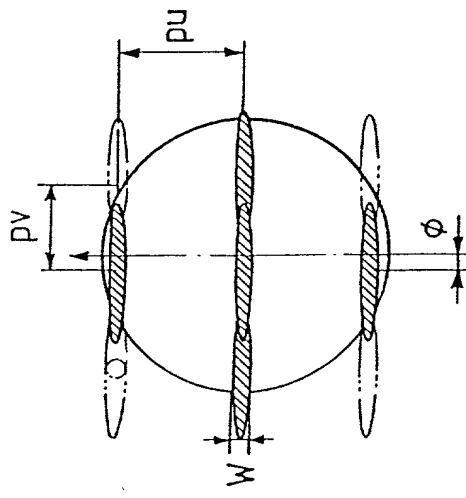


FIG. 31(a)

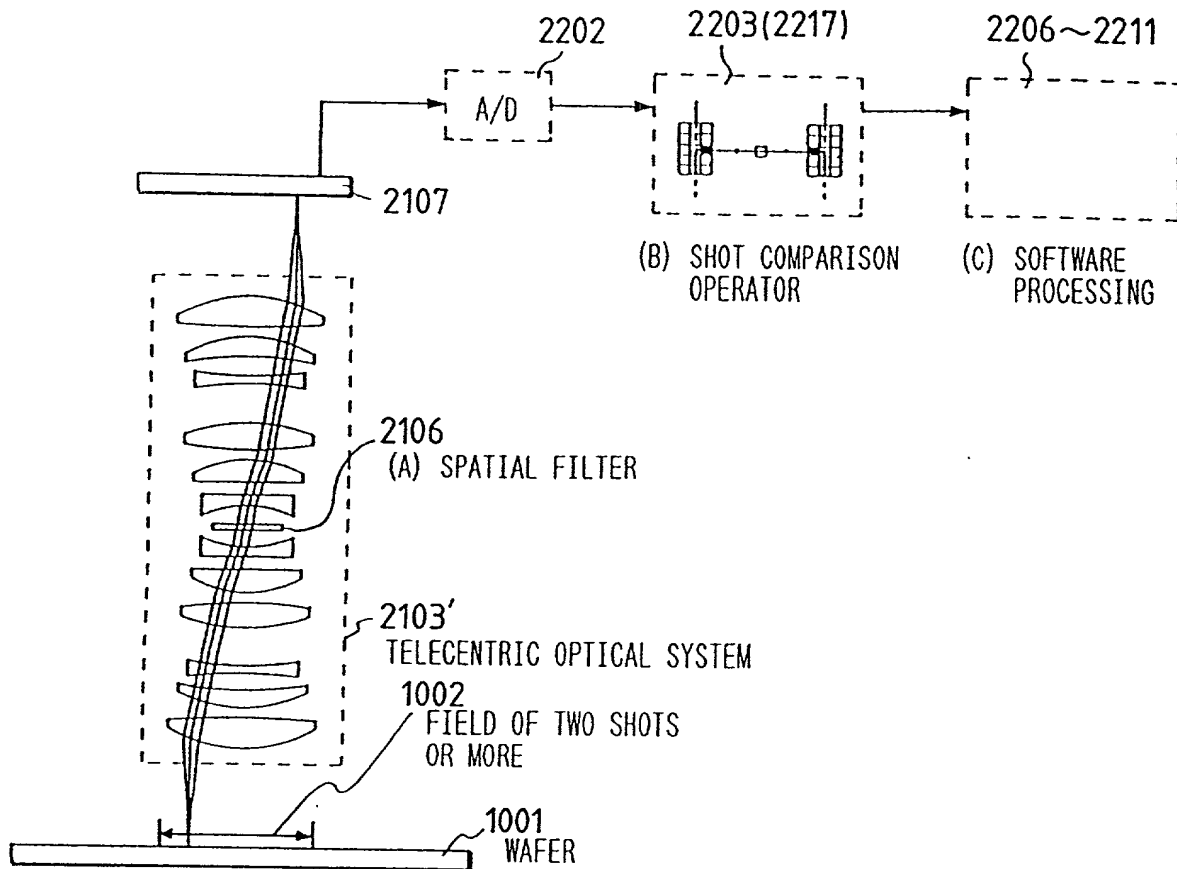
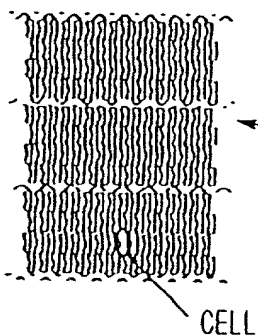


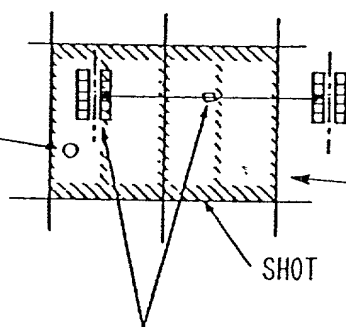
FIG. 31(b)(1)



(1) ERASING OF
PATTERN USING
SPATIAL FILTER

ERASE THE
REPEATABILITY
OF CELL USING
SPATIAL FILTER

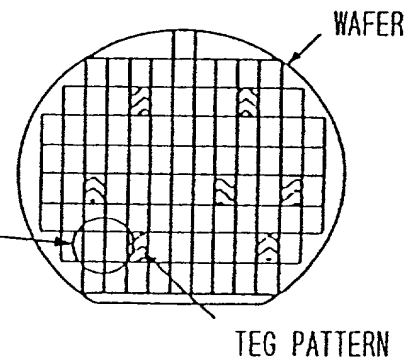
FIG. 31(b)(2)



(2) ERASING OF
PATTERN USING
SHOT COMPARISON
OPERATOR

ERASE USING THE
REPEATABILITY
OF TWO SHOTS

FIG. 31(b)(3)



(3) ERASING OF
TEG PATTERN
USING
SOFTWARE

ERASE USING
COORDINATE-
MATRIX DATA

FIG. 32

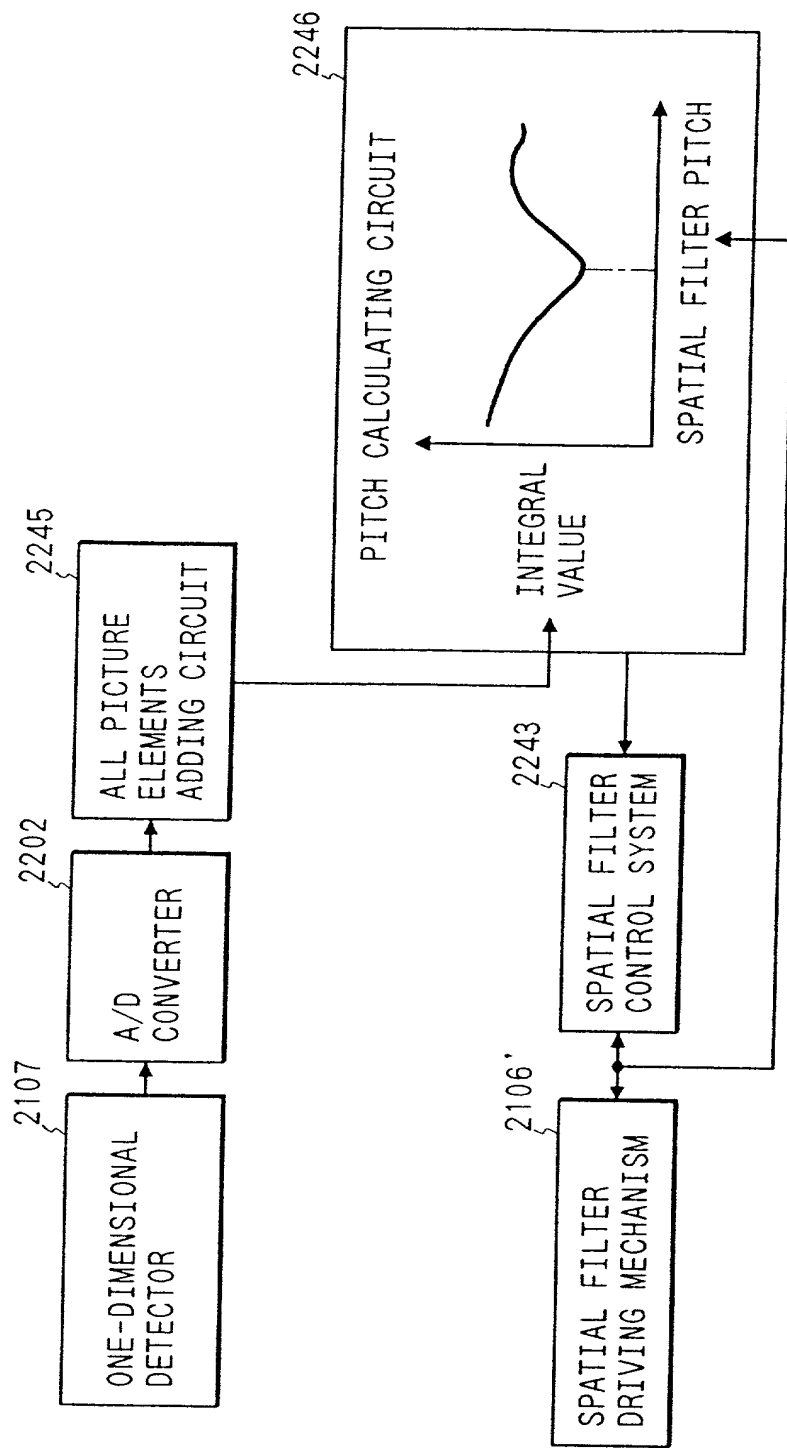


FIG. 33(a) is a schematic diagram of an optical system 2103' according to an embodiment of the present disclosure. The optical system 2103' includes a first lens group 2111 and a second lens group 2110. The first lens group 2111 includes a first lens 2111a, a second lens 2111b, and a third lens 2111c. The second lens group 2110 includes a fourth lens 2110a, a fifth lens 2110b, and a sixth lens 2110c. The optical system 2103' is configured to focus light from a light source 2103 onto a target 2104.

FIG. 33(a)

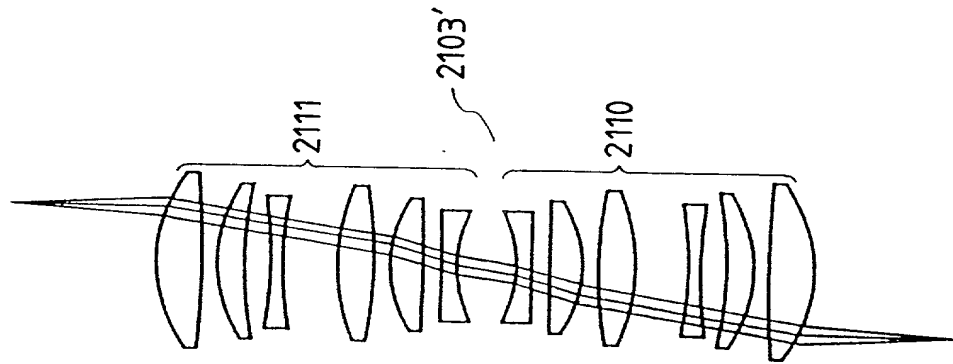


FIG. 33(b)

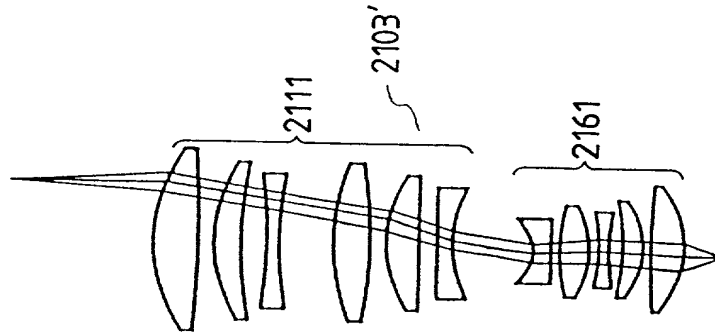


FIG. 34(a)

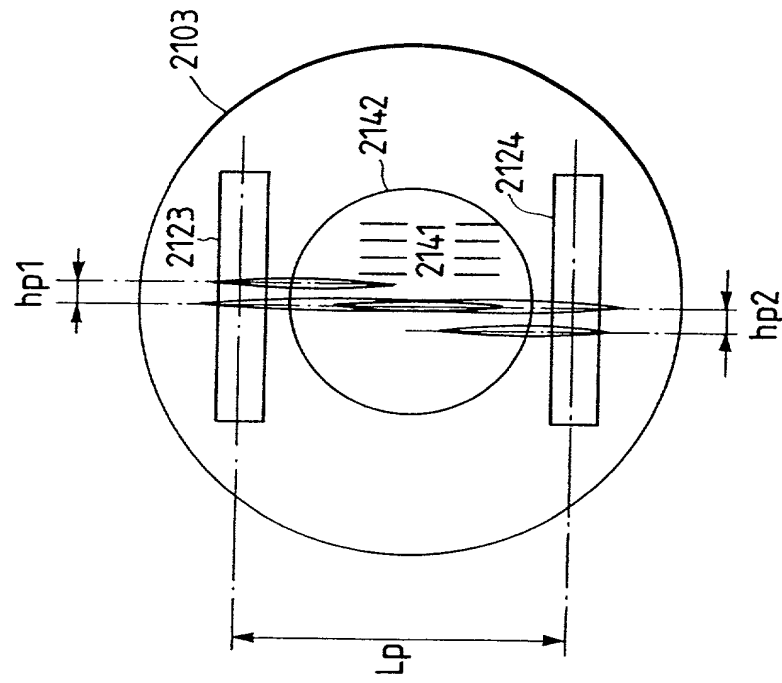


FIG. 34(b)

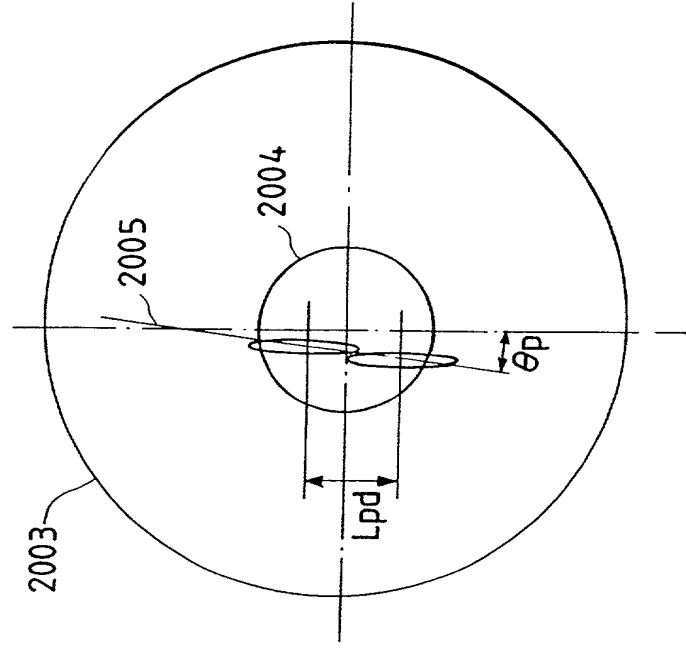


FIG. 35

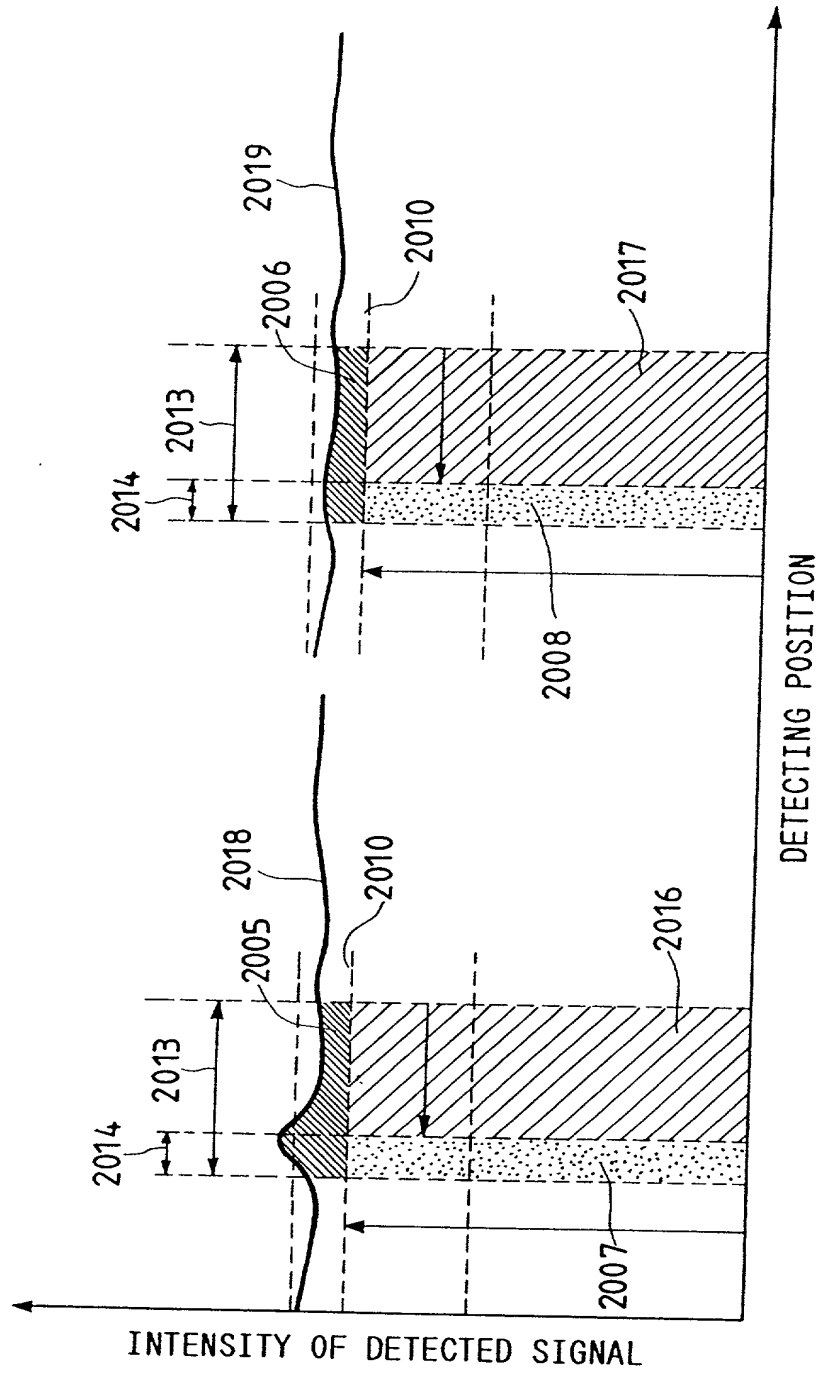


FIG. 36

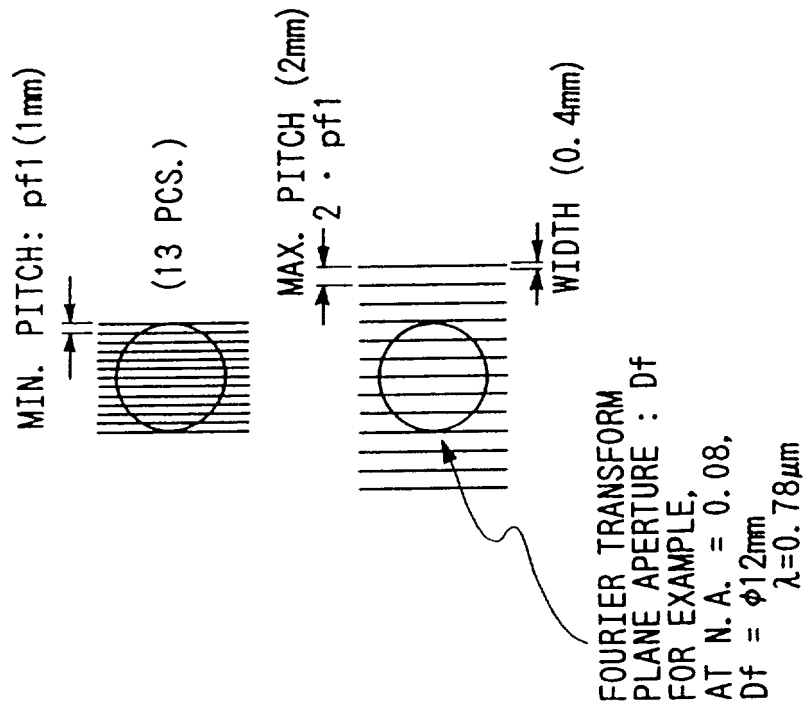


FIG. 37

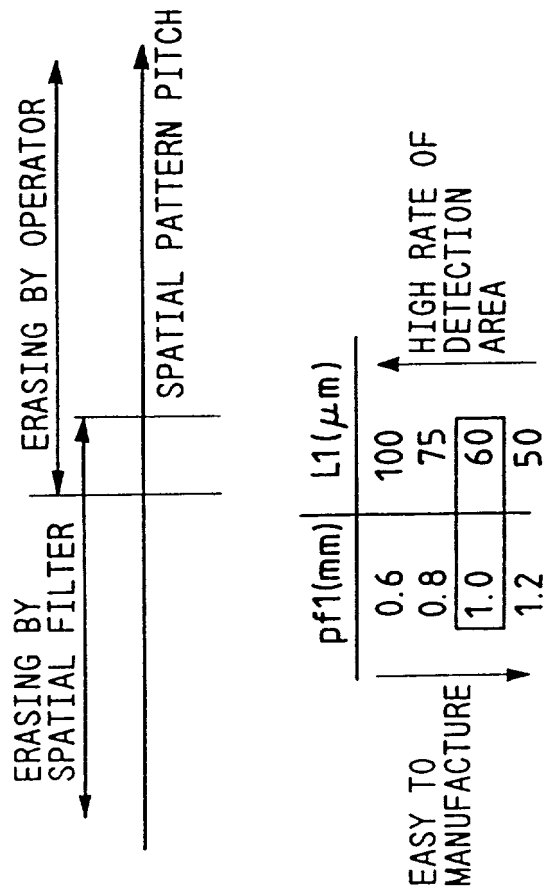


FIG. 38

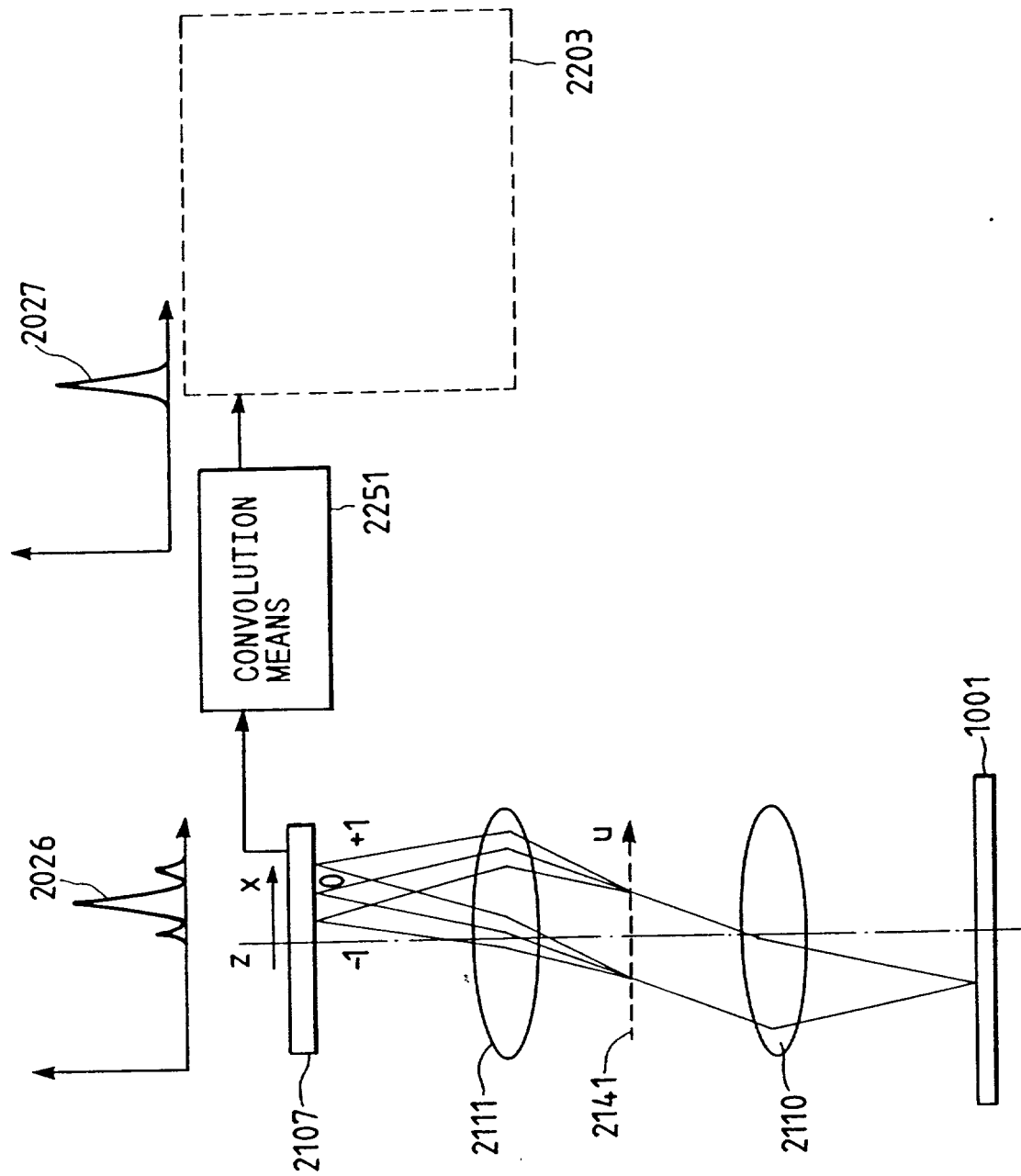


FIG. 39A

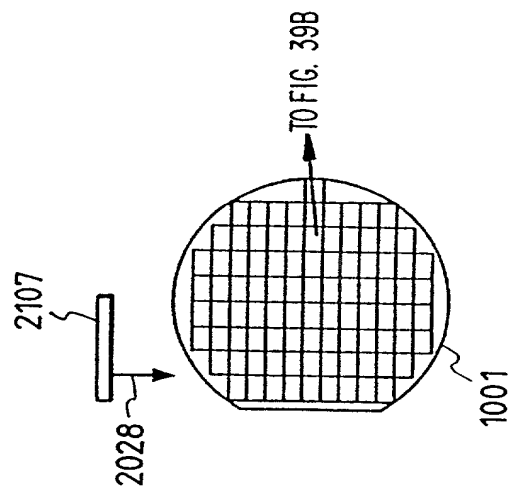


FIG. 39B

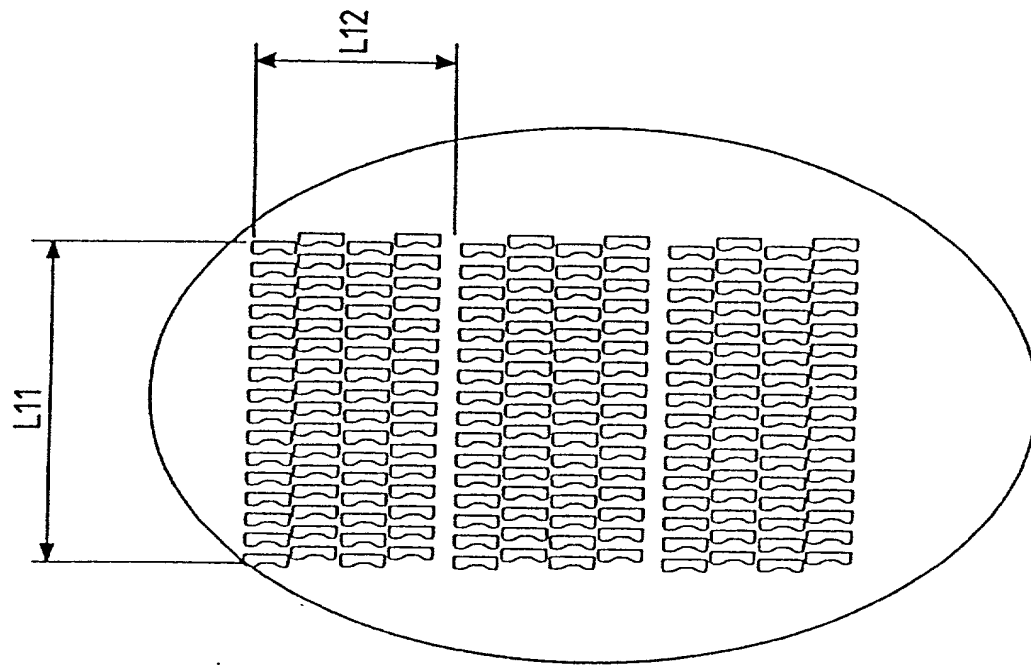


FIG. 40

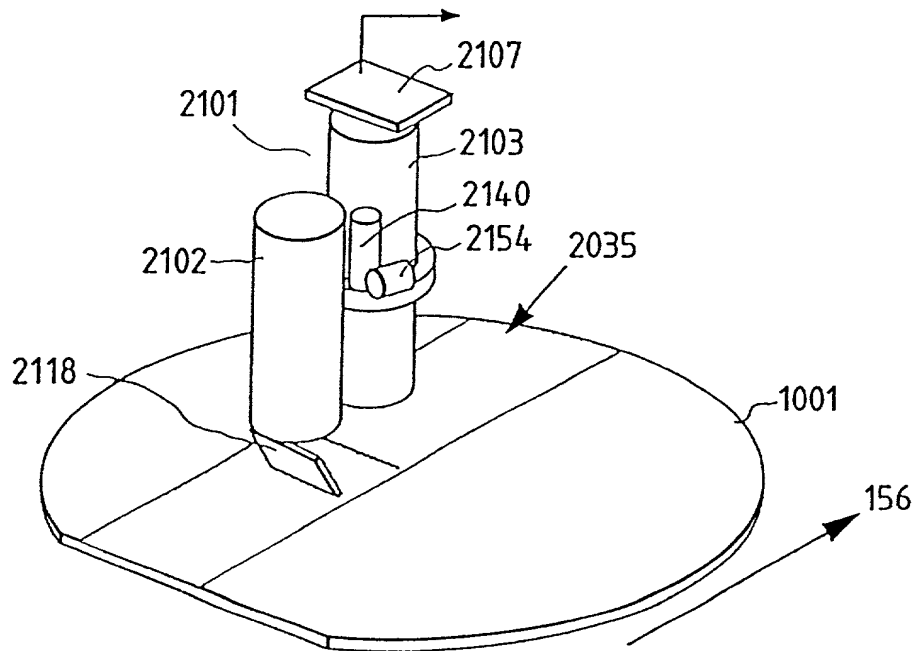


FIG. 41

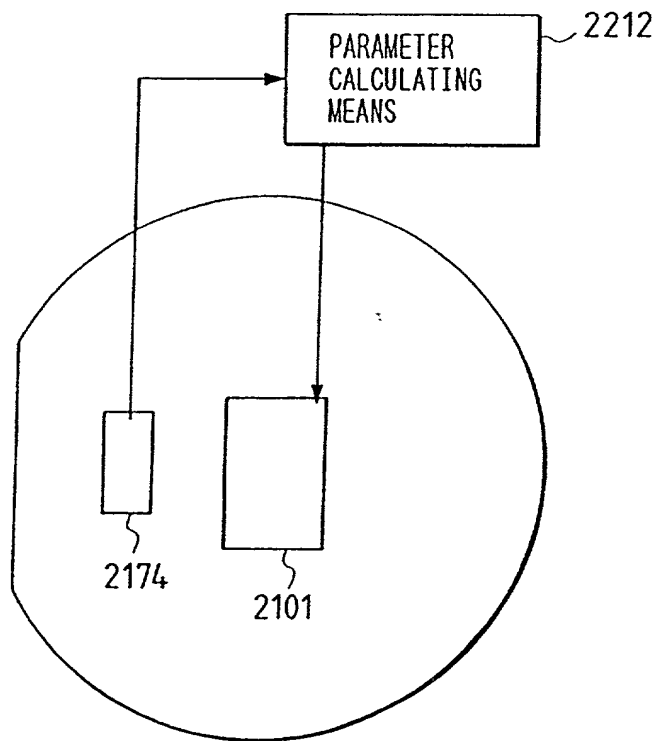


FIG. 42(a)

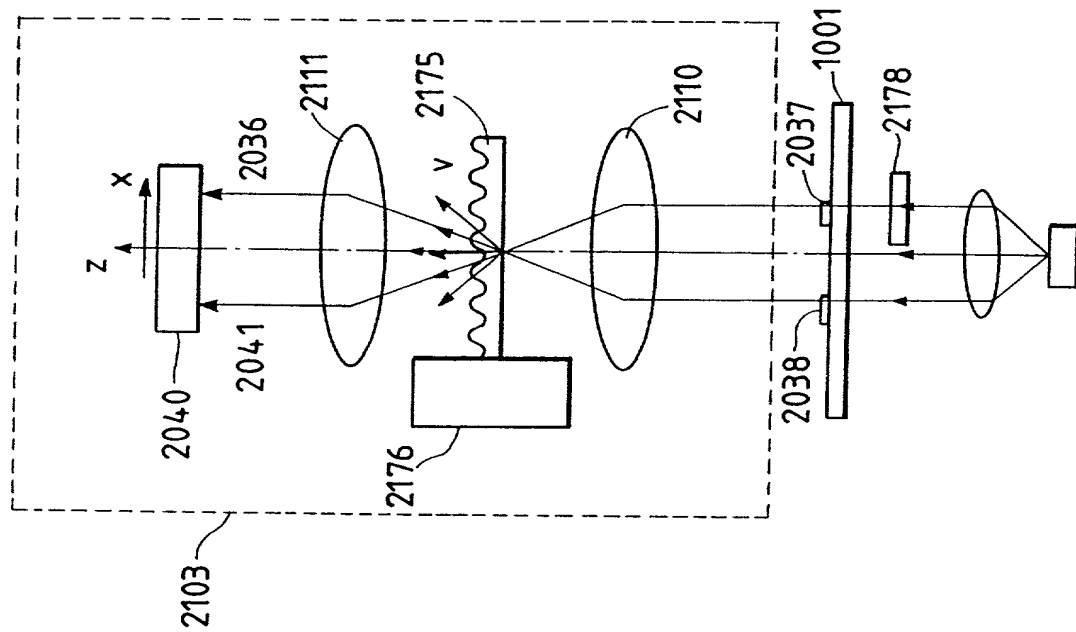


FIG. 42(b)

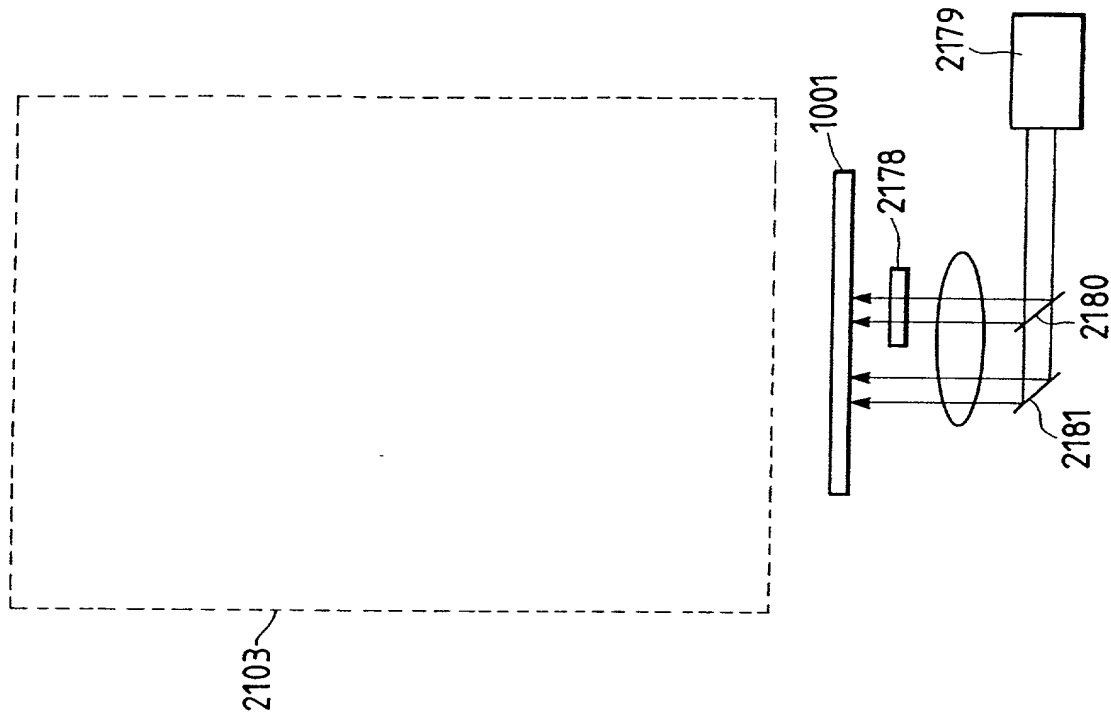


FIG. 43

